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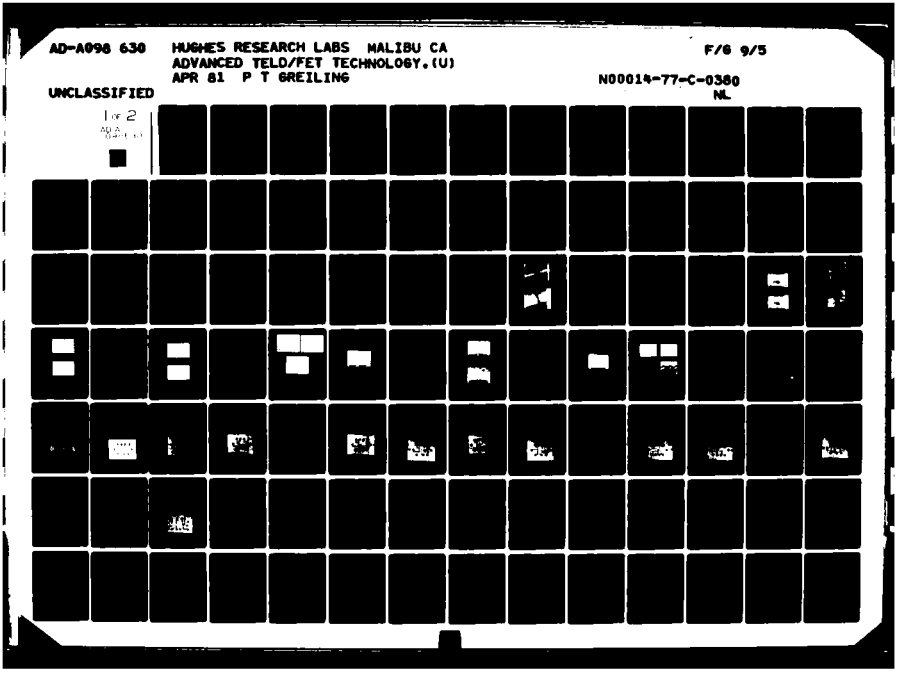

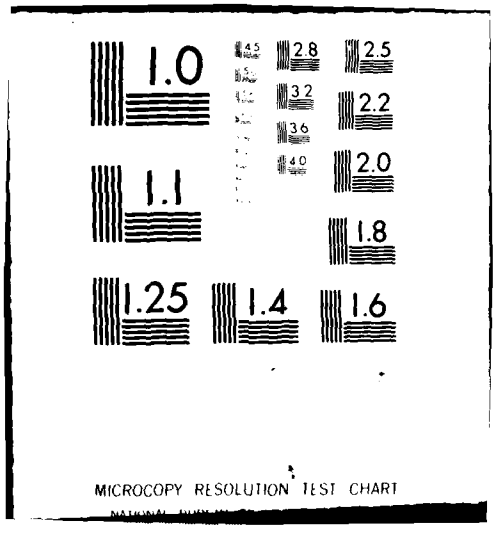
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LEVEL II

ADVANCED TELD/FET TECHNOLOGY

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Malibu, CA 90265

April 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Planar TELDs have been designed, fabricated, and tested. Computer models have been developed for designing and predicting the characteristics of TELDs as a function of device geometry, material parameters, and bias conditions. TELDs have been fabricated on ion-implanted LPE and VPE GaAs. Frequency dividers that divide the input signal by any integer from two through nine have been realized. A process technology for fabricating →

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TELD/FET circuits was developed and test circuits were fabricated incorporating this technology. Because of the relatively low doping density requirements for TELDs, material reproducibility was not sufficient to obtain repeatable results and the current drop was not satisfactory for successful operation of the circuits.

TABLE OF CONTENTS

SECTION I

Introduction

The objectives of this exploratory development program were: (1) to design and fabricate transferred-electron logic devices (TELDs), (2) to evaluate the dc and rf operating characteristics of the TELDs, and (3) to correlate the measured operating characteristics with a theoretical analysis. The device structures were fabricated using both ion-implanted and epitaxial GaAs material.

A mask set containing TELDs was designed in the initial phase of this program in order to investigate the operating characteristics of TELDs. Experimental data were obtained and used to determine design rules. The second phase of the program involved the design, fabrication and evaluation of more complex TELD/FET circuits. A process schedule was developed for fabricating 1 μm and 0.5 μm long gates for both TELDs and FETs on epitaxial and selectively ion-implanted GaAs wafers. The I-V characteristics of the TELDs processed in the second phase of the program exhibited a current drop of less than 10% which for the TELD/FET circuits is not large enough for proper operation.

A discussion of the device analysis, device and circuit design, TELD processing and device evaluation is presented in the following sections.

II. TELD DESIGN

A. Introduction

There are several design constraints based on material parameters and device geometry which determine the operation of TELDs. Referring to Figure 2-1, the affects of doping density, N_d, the gate-to-anode-spacing, ℓ_{gA}, the channel thickness d_o, and the mobility μ on the frequency of operation f_o, the power dissipation P_d, and the fractional current drop K are discussed in this section. In addition a computer analysis of the TELD which calculates the electric field in the gate-to-anode channel as a function of device and circuit parameters is presented at the end of this section.

B. Doping Density X Gate-to-Anode Spacing Product

To ensure that a domain grows to maturity, the product of the doping density times the device length must be above a critical value[1];

$$N_d \ \ell_{gA} \geq 10^{13} \text{ cm}^{-2} \tag{2-1}$$

since for small N_d the negative dielectric relaxation time is too short for a domain to form in a transit time.

In order to determine the operating frequency of a TELD, the spacing between the gate and anode must be designed to correspond to the proper transit time. However, the transit time depends upon the material mobility which in turn is a function of the doping density. In addition, inequality (2-1) must be satisfied. In order to determine the relationship of these parameters, the following assumptions have been made. The relationship between the doping density and mobility is approximated by[2]

$$N_d = N_o \exp(-\mu/\mu_o) \tag{2-2}$$

where $N_o = 1.1 \times 10^{19} \text{ cm}^{-3}$ and

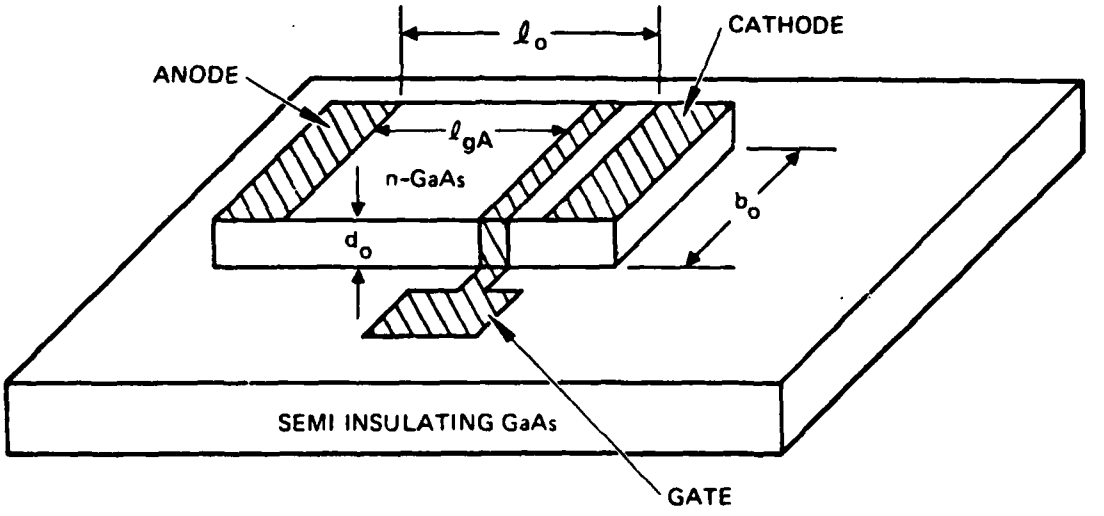


Figure 2-1. Planar structure of GaAs TELD

$$\mu_o = 826 \text{ cm}^2/\text{V-sec}$$

In order to achieve a mature domain

$$N_d \, \ell_{gA} \geq 10^{13} \text{ cm}^{-2} \tag{2-1}$$

thus

$$\ell_{gA} \, N_o \exp(-\mu/\mu_o) \geq 10^{13} \tag{2-3}$$

or

$$\mu \leq \mu_o \, \ell n \left(\frac{\ell_{gA} \, N_o}{10^{13}} \right) \tag{2-4}$$

The factor 10^{13} could be increased to assure large domains. From Claxton's work[3]

$$\ell_{gA} = \frac{1.26 \times 10^7 \cdot \mu}{f_o \cdot 8000} \tag{2-5}$$

where f_o = the operating frequency.

Thus

$$\ell_{gA} \leq \frac{1.26 \times 10^7 \, \mu_o \, \ell n}{f_o \cdot 8000} \left(\frac{\ell_{gA} \, N_o}{10^{13}} \right) \tag{2-6}$$

which is solved by selecting f_o and solving for ℓ_{gA}. These results are plotted in Figure 2-2. The experimental data point corresponds to a planar TED (two terminal) fabricated on 2 μm thick epitaxial GaAs with a doping density of 2×10^{16} cm^{-3} and a cathode-to-anode spacing of 30 μm.

C. Doping Density X Thickness (Width) Product

The energy stored in the electric field in the domain must be above a critical value which leads to the inequalities[4]

$$N_d \, d_o \geq 10^{12} \text{ cm}^{-2} \tag{2-7}$$

and

$$N_d \, b_o \geq 10^{12} \text{ cm}^{-2} \tag{2-8}$$

where b_o is the width and d_o is the thickness of the active device. The inequality imposes a severe limitation on fabricating TELDs by

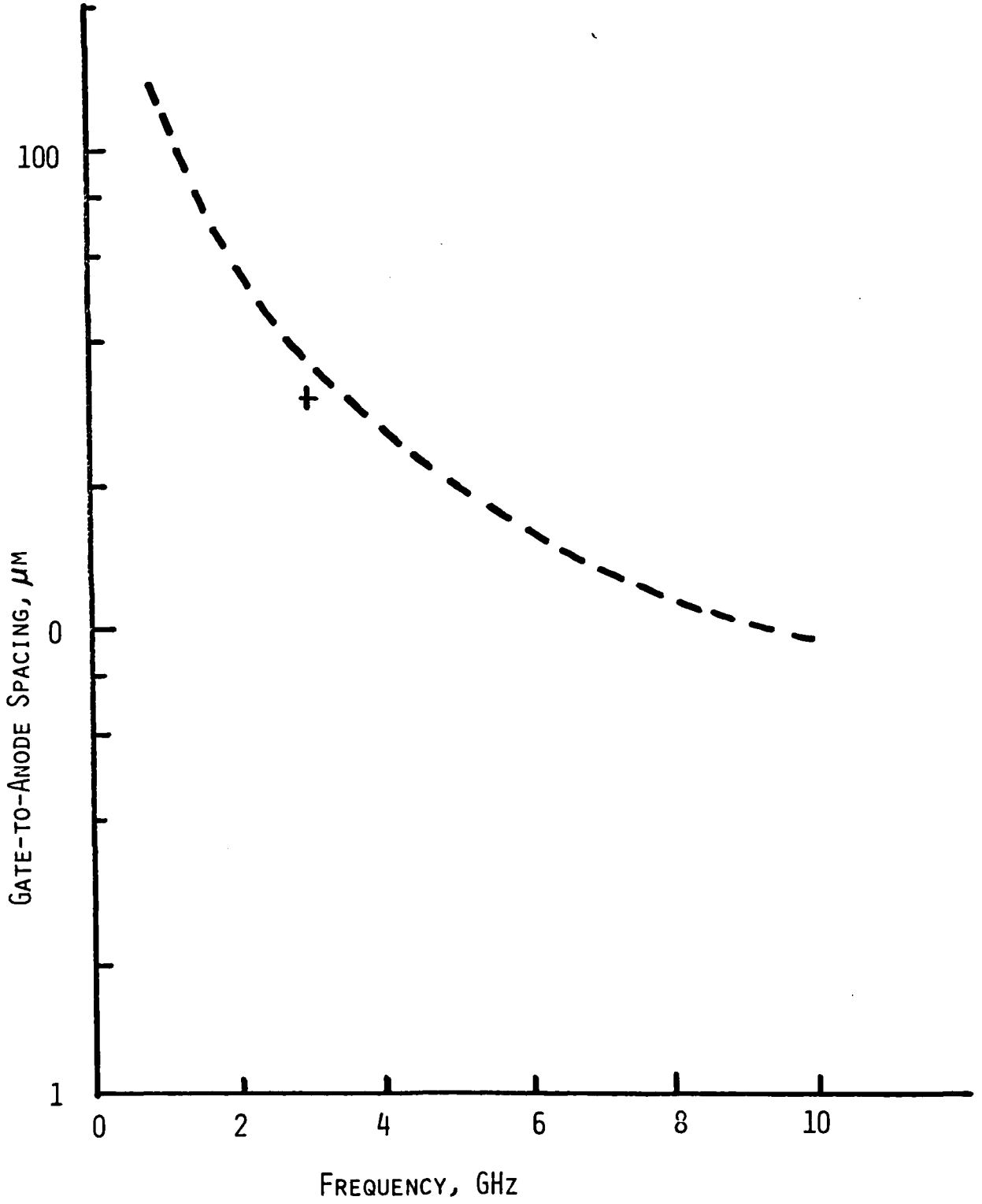


Figure 2-2. Gate-to-Anode spacing Operating vs Frequency

ion implantation, II, since for our II apparatus, the implant energy is limited to 550 keV for doubly ionized implants and 275 keV for singly ionized implants. Thus as shown in Figure 2-3, the maximum range for Si implanted into GaAs is approximately 0.5 μm.

D. Dependence of Current Drop on Mobility and Doping Density

The current drop is a function of the ratio of the peak velocity to the saturated drift velocity of electrons and is given by

$$K = \frac{v_p - v_s}{v_p} . \tag{2-9}$$

Kroemer[5] developed a velocity-field relationship for GaAs which is given by

$$v = \frac{\mu E + v_s \left(\frac{E}{E_{th}}\right)^4}{1 + \frac{E}{E_{th}}} \tag{2-10}$$

where v_s = saturated drift velocity

and E_{th} = threshold field.

Combining this relationship with Eqs. 2-4 and 2-9 the current drop is given by

$$K = \frac{1 - v_s/(E_{th}\ \mu_o\ \ell n\ N_o/N_d)}{1 + v_s\ (E_{th}\ \mu_o\ \ell n\ N_o/N_d)} \tag{2-11}$$

Using a saturated drift velocity of $.96 \times 10^7$ cm/sec and a threshold field[6] of 3.9×10^3 V/cm, the current drop K is plotted in Figure 2-4 as a function of doping density. In order to satisfy the inequality 2-7,

$$N_d\ d_o = 2 \times 10^{12}\ cm^{-2} \tag{2-12}$$

has been assumed and two thicknesses are labeled in the plot to show the maximum current drop predicted as a function of device thickness. As will be shown by our experimental results, this curve is optimistic in predicting the value of current drop.

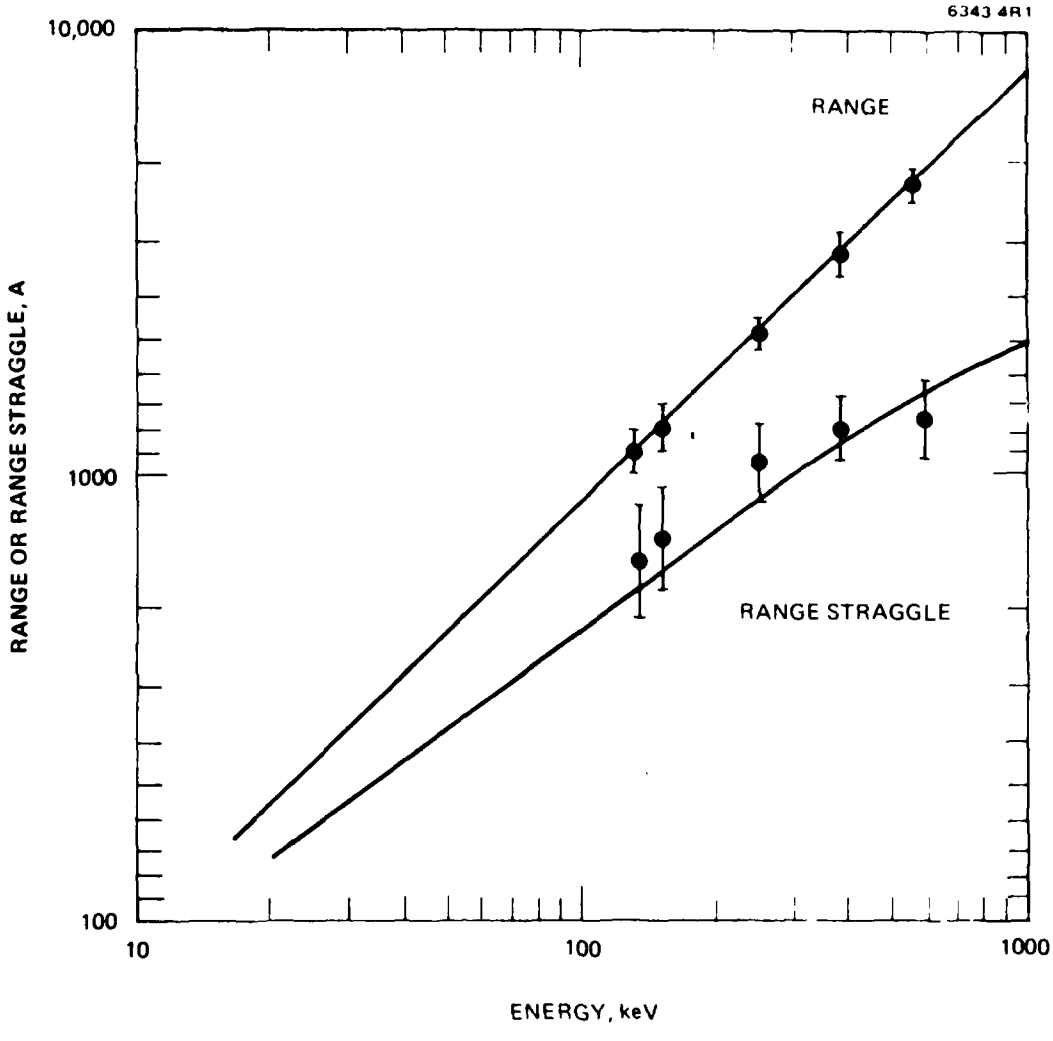


Figure 2-3. Range and range straggle for Si → GaAs.

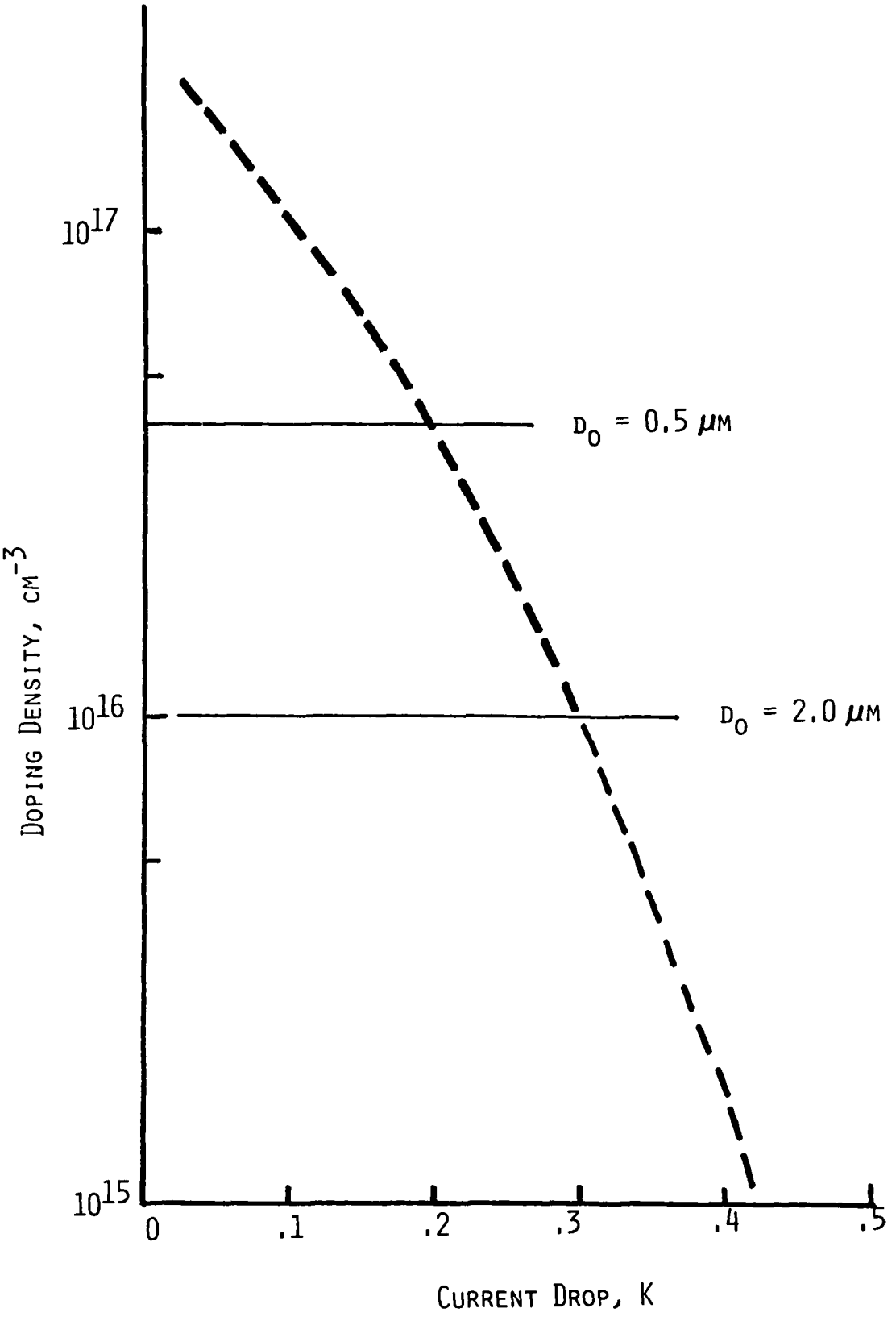


Figure 2-4. Current drop as a function of doping density.

E. Maximum Doping Density Limitation

An upper bound on doping density results from impact ionization occurring in the high-field region of the domain. As the doping density increases, domain growth time decreases, domain voltage increases, and the field in the domain increases. For large fields, electron-hole pairs are generated by impact ionization. Since the holes are trapped, the excess electrons will be localized at the trapped holes, thereby causing an apparent increase in the number of conduction electrons in this region. For each domain transit, the valley current is increased until domain formation becomes noncoherent. To prevent impact ionization occurring in the domains, the doping density should be limited[6] to less than 5×10^{16} cm^{-3}. However, since this restriction is based on a dc analysis for breakdown and impact ionization is time dependent and there is a time delay in the formation of the domain, this limit could be somewhat exceeded, possibly as high as 1×10^{17} cm^{-3}.

A second limitation on the doping density is the power dissipation of the device since as the doping density increases the current increases. Using Eq. 2-4, the power dissipated is proportional to the doping density in the following manner

$$P_d \propto \mu_o \ln\left(\frac{N_o}{N_d}\right) N_d$$

thus in order to minimize the power dissipation, N_d is selected as the minimum value which satisfies the inequalities (2-1) and (2-7).

F. TELD Model

A computer model has been developed that calculates the electrical characteristics of the TELD as a function of the device parameters and bias conditions (Appendix A). The calculation of the

threshold conditions follow the FET model by Pucel et al.[7] This same model has been used to derive the threshold conditions under the gate of the TELD. The analysis calculates the electric field under the gate and in the channel between the gate-cathode and gate-anode before and after threshold. Once the field under the gate exceeds the threshold value, the program calculates the steady-state conditions in the device assuming a mature domain has formed and is traversing the distance from the gate to the anode. The program calculates the electric field throughout the device, the current decrease caused by domain formation, and the voltage across both the device and a load resistor. The effect of doping density, channel depth, and load resistance can be investigated.

The electric field in a TELD with a mature domain in transit can be derived if the velocity (v) versus electric field (E) characteristic is known. Following the derivation of Hartnagel[8] in which a piecewise linear approximation for the v versus E curve is assumed as shown in Figure 2-5, one can show that for $E_M < E_S$

$$(E_t - E_R)^2 \mu_o + (E_p - E_t)^2 \mu_n = (E_S - E_p)^2 \mu_n + 2 (E_S - E_p) (E_M - E_S) \mu_n \qquad (2\text{-}13)$$

and for $E_M > E_S$

$$(E_t - E_R)^2 \mu_o + (E_p - E_t)^2 \mu_n = (E_M - E_p)^2 \mu_n. \qquad (2\text{-}14)$$

These equations are based on the assumption that a mature domain has formed and, therefore, that the equal-areas rule applies. Eq. 2-13 has a factor of 2 which Hartnagel[8] does not show. From Figure 2-5, one can show the following relations:

$$(E_p - E_t) \mu_n = (E_t - E_R) \mu_o \qquad (2\text{-}5)$$

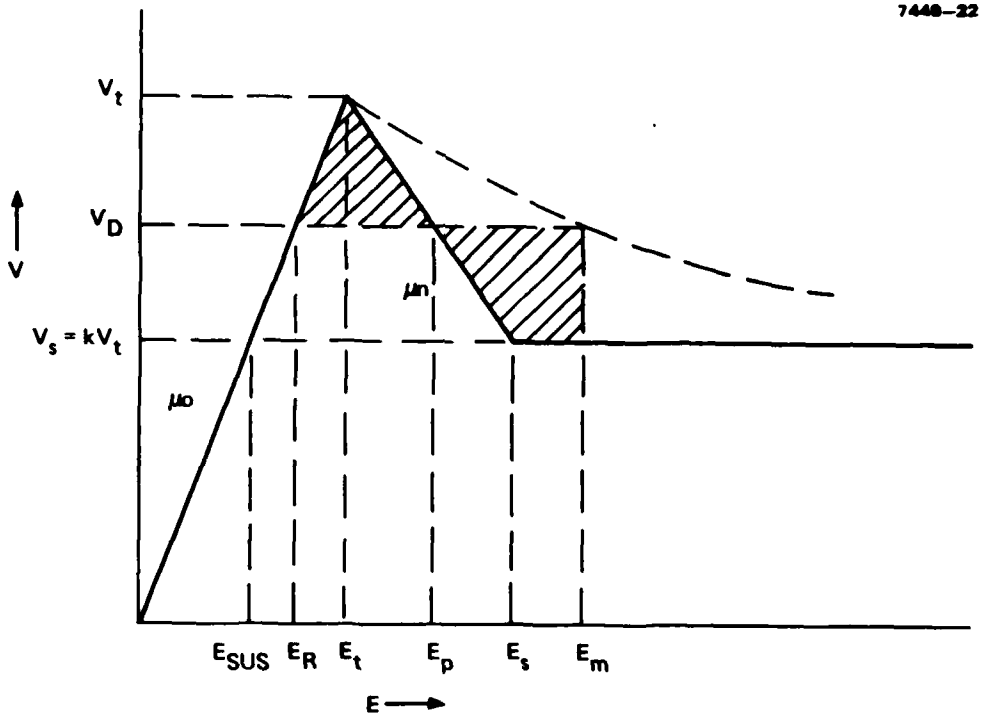


Figure 2-5. Piecewise linear approximation to the velocity versus electric field for GaAs.

$$E_S = E_t = v_t \frac{(1-k)}{\mu_n} \tag{2-16}$$

$$v_t = \mu_o E_t \cdot \tag{2-17}$$

After some manipulation, Eqs. 2-13 and 2-14 can be reduced to

$$(E_M - E_R) = \frac{(E_t - E_R)^2 \left(1 + \left(\frac{\mu_o}{\mu_n}\right)\right)}{2(E_R - kE_t)} - E_R \left(1 + \frac{\mu_o}{2\mu_n}\right) + E_t \left(1 + \frac{\mu_o}{\mu_n}\left(1 - \frac{k}{2}\right)\right) \tag{2-18}$$

for $E_M > E_S$ and

$$E_M - E_R = (E_t - E_R) \left[\left(\frac{\mu_o}{\mu_n}\left(1 + \frac{\mu_o}{\mu_n}\right)\right)^{1/2} + \left(1 + \frac{\mu_o}{\mu_n}\right)\right] \tag{2-19}$$

for $E_M < E_S$.

Using Eq. 2-18 or 2-19, the domain voltage is obtained from

$$V_D = \frac{\varepsilon (E_M - E_R)^2}{2 q N_D} \tag{2-20}$$

With the corrected version of the domain voltage, the steady-state conditions for a TELD with a domain in transit are calculated. Assuming a circuit similar to that shown in Figure 2-6, the current is related to the voltage by

$$V_{Bias} = IR_L + V_{TELD}, \tag{2-21}$$

where $V_{TELD} = V_D + V_{gate} + E_R (\ell_{Ag} + \ell_{Cg})$. (2-22)

The distances from gate-to-anode and from gate-to-cathode are given by ℓ_{Ag} and ℓ_{Cg}, respectively. The voltage drop from the anode side to the cathode side of the gate is given by V_{gate} and is calculated by the Pucel[7] model. In addition, the current through the TELD must satisfy

$$I = q \mu_o N_D E_R b_o d_o, \tag{2-23}$$

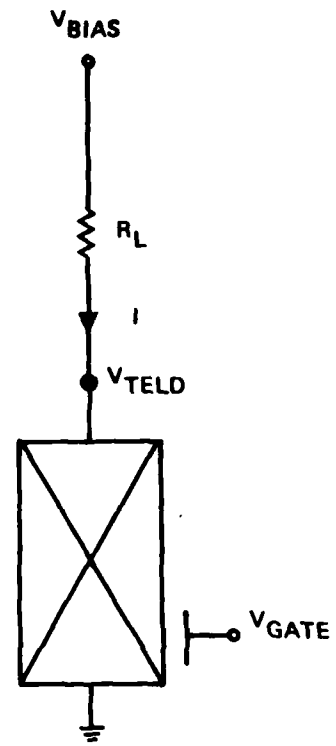


Figure 2-6.
Circuit for TELD and load resistor.

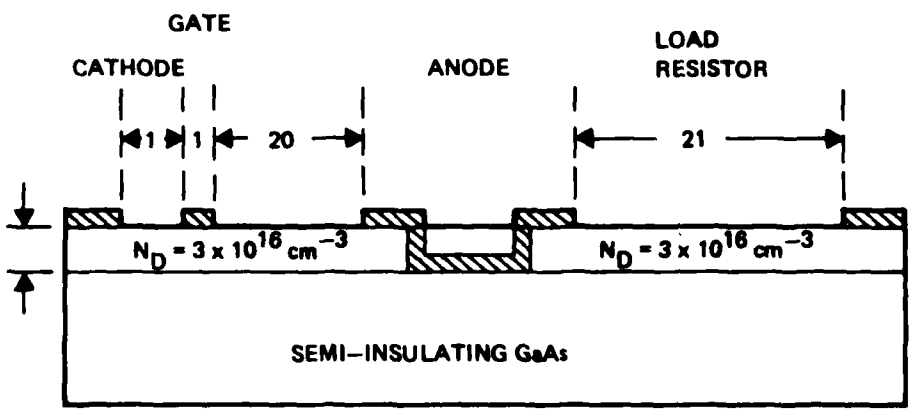


Figure 2-7. Schematic of TELD and load resistor (μ_n = 6000 cm^2/V-S, E_T = 3.2 x 10^3 V/cm) (dimensions in micrometers).

where $b_o d_o$ is the channel cross sectional area. Thus, to determine the steady-state condition for a given bias voltage V_{Bias}, load resistor R_L, and gate bias V_{gate} which is a function of the bias applied to the gate, a self-consistent solution must be found for Eqs. 2-18 through 2-23. In comparison, before the domain is triggered, the conditions to be satisfied are

$$V_{Bias} = I' R_L + V'_{TELD} \tag{2-24}$$

$$V'_{TELD} = V'_{gate} + E'_R (\ell_{Ag} + \ell_{Cg}) \tag{2-25}$$

$$I' = q \mu_o N_D E'_R b_o d_o. \tag{2-26}$$

A computer program was written to solve these two sets of equations. The results of the program for the TELD and R_L shown in Figure 2-7 are given in Table 2-1. The program calculates the conditions in the circuit before and after domain formation with a variable bias voltage that just satisfies the threshold condition for the given gate bias.

This model predicts a large current drop back since a mature domain is assumed to form immediately, resulting in a low value for the sustaining field in the drift region of the TELD. For the domain, which is nucleated under the gate, to transit from the gate to the anode, the field in this region must be large enough to sustain the domain. A first-order approximation to the sustaining field is that the current density in this region is greater than that obtained for saturated drift velocity of the carriers. Referring to Figure 2-5, this implies that the field is greater than E_{sus} since

$$J = qN_D\mu \quad E > qN_D v_{sat} \tag{2-27}$$

or

$$E > \frac{v_{sat}}{\mu} = E_{sus} \tag{2-28}$$

As the channel thickness decreases, the domain is nucleated under the

gate for smaller and smaller V_{gC} and V_{AC} with lower and lower fields between the anode and the gate. For very thin channels (i.e., $\leq$ 0.5 μm), the field in the drift region is not above the sustaining value and a domain will not propagate. This implies that, for a given Schottky-barrier height and channel doping density, there is a minimum channel thickness. If the depletion region X is normalized to the channel thickness, d_o, then a maximum value for X/d_o is obtained as a function of doping density.

Table 2-1. TELD Current and Voltage Before and After Domain Formation (R_L = 182 Ω, N_D = 3 x 10^{16} cm^{-3}, d_o = 2 μm, b_o = 20 μm)

V_{Bias}, V	V_{gC}, V	V_{TELD}		ΔV, V	I, mA		ΔI, mA	K
		Before	After		Before	After		
12.03	0	6.16	8.62	2.96	32.25	18.76	13.49	0.42
11.51	-1	5.90	8.09	2.19	30.82	18.78	12.04	0.39
11.12	-2	5.70	7.69	1.99	29.75	18.79	10.96	0.37
10.39	-4	5.34	6.96	1.62	27.72	18.83	8.89	0.32
9.81	-6	5.06	6.38	1.32	26.13	18.87	7.26	0.28

The calculated value for the current drop are larger than the values predicted in Figure 2-4 due to the simplified and optimistic price-wise linear velocity-field relationship assumed in Figure 2-5.

In addition to the requirements on the device geometry and material parameters determined by the model, the sensitivity of the field under the gate to the gate bias is also obtained. Trigger sensitivity is an important design and performance parameter in the operation of TELDs. Trigger sensitivity is defined as the minimum change of electric field required for domain formation due to a voltage applied to the gate. Sugeta et al.[9] defined the minimum field as that due to shot noise in the carrier density; however, as

pointed out by Upadhyayula,[10] this definition does not lead to a useful device, since one would not want the TELD triggered by noise. Upadhyayula derived the trigger sensitivity including the load resistor in the anode circuit and showed that it is increased by $(1 + g_m R_L)$ due to the load resistor since it provides positive feedback. As the gate voltage is made more negative, the depletion region under the gate increases, which causes a smaller cross-sectional area for the current. This decreases the current, which in turn decreases the voltage drop across R_L. Since the bias is constant, device voltage increases, which increases the field under the gate. Thus, the feedback increases the field towards threshold. For the case with a cathode follower circuit, the feedback is negative. The reverse bias on the gate, which determines the depletion width and therefore the current through the device, is the difference between the potential at the edge of the depletion region in the channel and the potential on the gate. Increasing the negative gate bias increases the reverse bias, which increases the depletion region. This in turn reduces the current and the voltage drop across the load resistor. As the voltage across R_L decreases, the cathode potential decreases. Thus, the potential of the depletion edge under the channel decreases, and the reverse bias between the channel and the gate decreases. Following the derivation of Upadhyayula, the current through the TELD is given by

$$I = (1 - X)\ \alpha E\ b_o d_o, \tag{2-29}$$

where α is conductivity.

The variation of field with gate voltage V_g is given by

$$\frac{dE}{dV_g} = \frac{E}{(1 - X)} \frac{dX}{dV_g} + \frac{g_m}{d_o b_o\ \alpha(1 - X)}, \tag{2-30}$$

where

$$g_m = \frac{dI}{dV_g}$$

The depletion width for a given potential drop ϕ is

$$Xd_o = \sqrt{\frac{2\varepsilon\phi}{qN_d}} \tag{2-31}$$

The potential drop for the two cases (anode load resistor, A, and cathode follower, CF) is

$$\phi_A = V_B - I(R_L + R_{gA}) - V_g + \phi_B \tag{2-32}$$

and

$$\phi_{CF} = \phi_B + I(R_L + R_{gC}) - V_g, \tag{2-33}$$

where

V_B = bias voltage

R_{gA} = anode-to-gate channel resistance

R_{gC} = cathode-to-gate channel resistance

ϕ_B = build-in potential.

Evaluating dX/dV_g and substituting into Eq. 2-30 yields

$$\left.\frac{dE}{dV_g}\right|_A = \frac{-E(1 + g_m\ (R_L + R_{gA}))}{(1 - X)\ 2X\phi_p} + \frac{g_m}{\sigma b_o\ d_o\ (1 - X)} \tag{2-34}$$

and

$$\left.\frac{dE}{dV_g}\right|_{CF} = \frac{-E\ (1 - g_m\ (R_L + R_{gC}))}{(1 - X)\ 2X\phi_p} + \frac{g_m}{\sigma b_o\ d_o\ (1 - X)}, \tag{2-35}$$

where ϕ_p is the pinch-off voltage.

Rearranging terms and using the relations $l_{gA}E = R_{gA}\ I - V_{gA}$ yields

$$\left.\frac{dE}{dV_g}\right|_A = -\frac{(1 + g_m R_L)\, E}{2X\,(1 - X)\,\phi_p} - \frac{g_m}{l_g}\left[R_{gA}\left(\frac{V_{gA}}{2X\,(1 - X)\phi_p} - 1\right)\right] \tag{2-36}$$

and

$$\left.\frac{dE}{dV_g}\right|_{CF} = -\frac{(1 - g_m R_L)\, E}{2X\,(1 - X)\,\phi_p} + \frac{g_m}{l_{ga}}\left[\frac{R_{gC}\, V_{gA}}{2X\,(1 - X)\phi_p} + R_{gA}\right]. \tag{2-37}$$

The last term in the parentheses in both equations is positive for most TELD designs and, therefore, dE/dV_g is negative for the load resistor in the anode circuit but can be either negative or positive for the cathode follower case. Thus, the trigger sensitivity for the cathode follower case is decreased by $(1 - g_m R_L)$.

The computer model calculates the trigger sensitivity indirectly since the electric field under the gate at the anode edge is calculated as a function of gate bias for a given bias condition, doping density, device geometry and load resistor. The electric field for the TELD described in Figure 2-7 with gate bias as a parameter is shown in Figure 2-8. Figure 2-9 plots the electric field under the gate at the anode edge as a function of the gate bias for this TELD and for a similar TELD with a doping density of 10^{16} cm^{-3}. The $N_d\, d_o$ and $N_d\, \ell_o$ product for the two devices is given in Table 2-2 along with the trigger sensitivity and the corresponding gate trigger voltage to increase the field by 0.1 E_T. An optimum value[11] for ΔV_g is between 0.5 and 1.5 V: if ΔV_g is too small it will trigger spontaneously and, if ΔV_g is too large it will take too much logic swing and energy from the input to trigger the device.

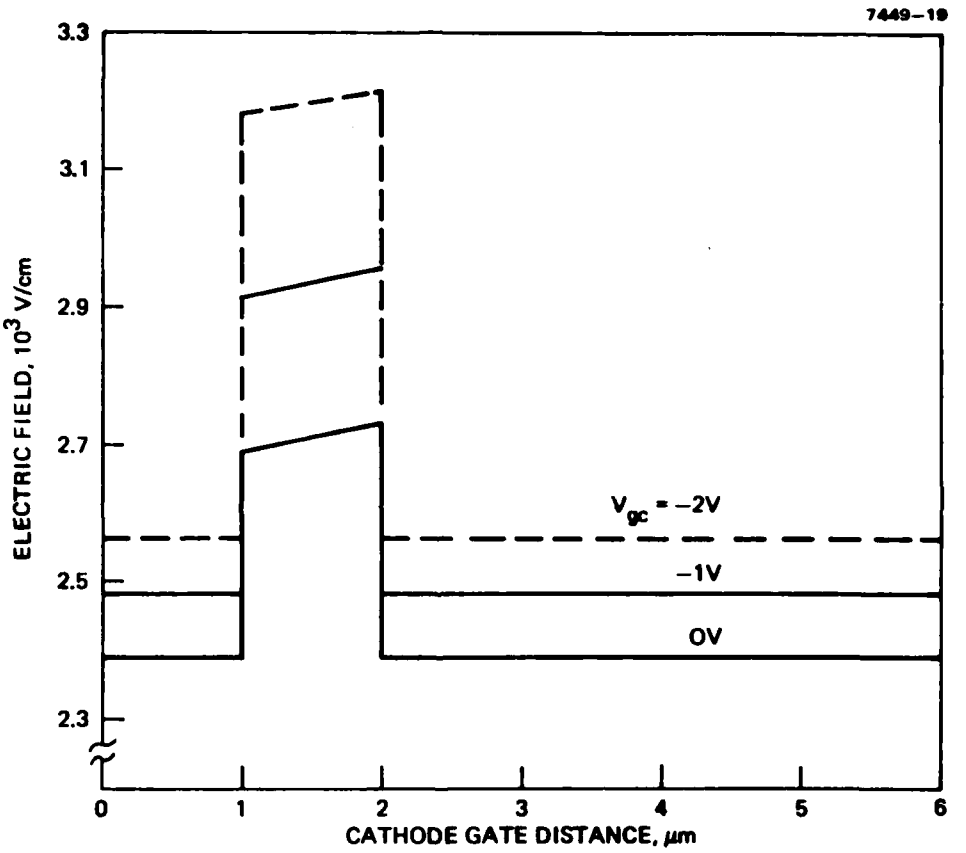


Figure 2-8. Electric field versus distance for TELD and load resistor in Figure 2-7 (V_{bias} = 11.1 V, I_{DS} = 29.75 mA).

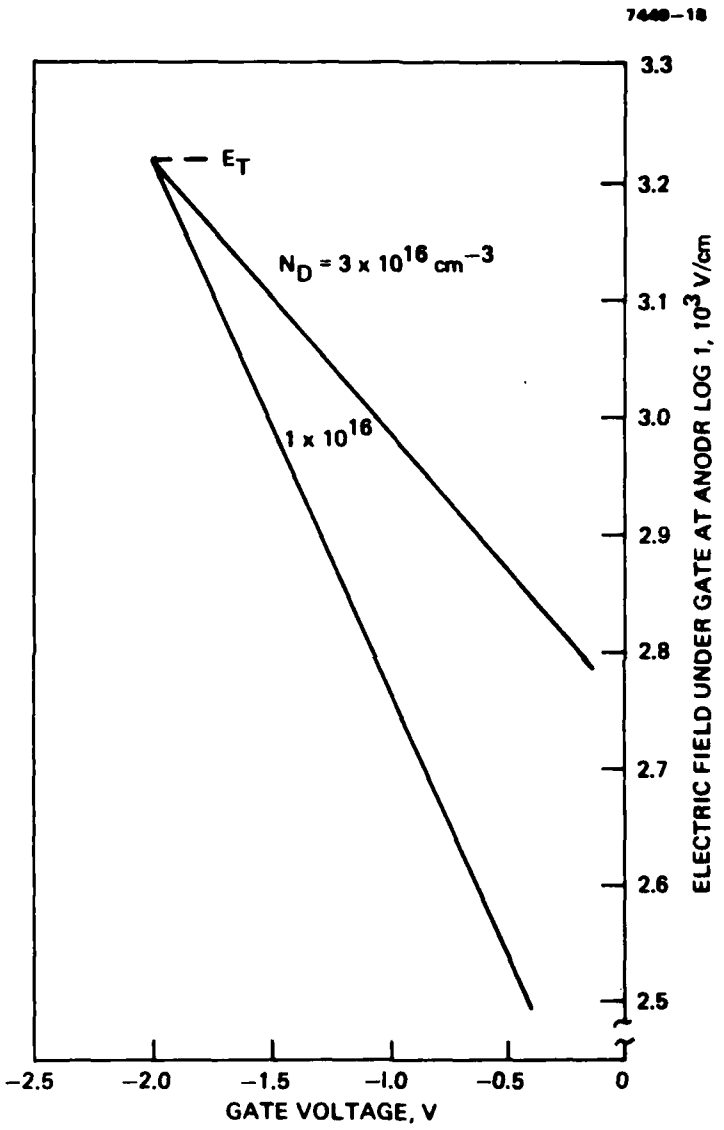


Figure 2-9. Electric field under the gate versus gate bias (R_L = 182 Ω, E_T = 3218 V/cm).

Table 2-2. TELD Trigger Sensitivity

Doping Density, cm^{-3}	$N_d d_o$, cm^{-2}	$N_d \ell_o$ cm^{-2}	$\Delta E/\Delta V_g$, cm^{-1}	ΔV_g, V
3×10^{16}	6×10^{12}	6×10^{13}	228	1.40
1×10^{16}	2×10^{12}	2×10^{13}	460	0.695

III. TELD FABRICATION

A. Introduction

A GaAs process technology for the fabrication of TELD/FET circuits was developed on this program. The new process is compatible with FET IC fabrication and incorporates as much of this technology as possible. Thus, the technology development part of the program concentrated on the areas which required novel processes. In this section the overall process is outlined and our effort to develop the new processing steps for the fabrication of TELD/FET circuits are discussed.

B. TELD/FET Process Steps

Starting with either epitaxial GaAs wafers or deeply implanted wafers, the process steps for fabricating TELD/FET circuits are summarized in Table 3-1. Typical epitaxial material had a doping density of 2×10^{16} cm^{-3} to 3×10^{16} cm^{-3} with a thickness of 2 μm. The ion-implanted wafers had a triple implant resulting in an active region of $\sim$ 0.5 μm deep and a peak doping density of $\sim 5 \times 10^{16}$ cm^{-3}. The mesa etch defines the TELD active areas, leaving the remainder of the wafer semi-insulating. The FETs were formed by selective implantation with a dose of 6×10^{12} cm^{-2} at 100 keV. The n^+ Ohmic contacts for both the TELDs and FETs are also selectively implanted and then the wafer is capped and annealed to activate the implants. Next, the Ohmic contacts are deposited, followed by the gate metal for the TELDs. At this point the threshold and drop back currents for the TELD are measured to determine the proper value for I_{DSS} of the FETs. The gate channels of the FETs are then etched to the desired depth to match the I_{DSS} of the FETs to the measured TELD current levels. The FET gate metal

is deposited next. The dielectric, either anodic oxide or SiO_2, for the capacitive pick-off gates is defined and the resistors in the circuits are etched to the proper value. The interconnect metal is deposited completing the process steps.

Table 3-1

Process Steps for TELD/FET Circuits

TELD Mesa
FET Mesa
Ohmic contacts
TELD gates
FET gates
Pick-off gate dielectric
Resistor trim
Interconnect metal

C. TELD Technology

Two areas of technology relating to TELD fabrication were pursued on this program: ion implantation and TELD fabrication with capacitive coupling to the next stage. The ion implantation experiments addressed the problems of forming relatively deep, and low doped profiles necessary for the transferred electron effect to be observed. The fabrication experiments focussed on the problems of generating narrow gate lines over relatively high mesa steps and deposition of the deielectric layer for capacitive coupling.

To observe significant current drop in TELDs, the doping thickness product $N_d d_o$ must be greater than 2×10^{12} cm^{-2}. With a 250 keV implant capability and double ionization, the maximum range

of implanted Si ions, as indicated in Figure 2-3, is 0.5 μm. The doping level must be greater than 4×10^{16} cm^{-3} to obtain significant current drop back (Figure 2-4). The doping level is also constrained below 10^{17} cm^{-3} to avoid impact ionization and above 3×10^{16} cm^{-3} to avoid unpredictable compensation by substrate impurities. Again from these considerations a doping level of 5×10^{16} cm^{-3} is an excellent choice.

Due to previously observed difficulties in obtaining good activation with low concentration implants in GaAs, we performed three sets of experiments to investigate the influence of ion source, ion dose and anneal temperature on the implant characteristics. In all experiments the energy used was 550 keV which is the maximum achievable energy with double ionization in our 275 keV implant machine. All implanted layers were capped with CVD SiO_2 deposited at 420°C and annealed in forming gas atmosphere for 20 minutes. The resulting active layer characteristics were evaluated with the standard material evaluation pattern.

To evaluate different implant sources both silicon tetraflouride (SiF_4) and Silane SiH_4 were used as the ion source. The results of these comparative experiments are shown in Table 3-2. The SiH_4 implant gave a somewhat higher than the normally expected activation of 50 to 60%. Further investigation of the characteristics indicates the possibility of surface conversion.

One of the problems with the use of silicon implantation is the possibility of nitrogen contamination (Si^+ has the same e/m ratio as N_2^+). To check for this possibility a series of singly ionized 275 keV implants were performed using both mass 28 silicon and mass 29 which should be free of N_2 contamination. These results are

Table 3-2

Comparison of Ion Sources for TELD Implants. (Dose = 3.5×10^{12} cm^{-2}, Energy = 550 keV, anneal 860°C)

Ion Source	Mobility (cm^2/V·sec)	Sheet Resistance	% Activation
$SiF_4{}^{28}$	4528	760	53
$SiH_4{}^{21}$	4901	580	74

summarized in Table 3-3. With the exception of the $SiH_4{}^{29}$ experiments,

Table 3-3

Comparison of Si ion mass and anneal temperatures (dose = 3.5×10^{12} cm^{-2}, Energy = 275 keV)

Ion Source	Mobility (cm^2/V·sec)	Sheet Resistance ohms/square	Percent activation	Anneal temperature (°C)
$SiH_4{}^{29}$	3600	940	48	800
$SiH_4{}^{29}$	5300	1100	---	860
$SiH_4{}^{28}$	3225	880	60	800
$SiH_4{}^{28}$	3765	660	71	860
$SiF_4{}^{28}$	3500	920	51	800
$SiF_4{}^{28}$	3805	560	80	860

all results of this experiment were as expected with higher anneal temperatures giving higher activation and higher mobility. Note, however, the mobilities in this rather heavily chromium doped substrate are rather low and thus such material would produce marginal TELDs at best. It was observed that the doping profiles from the two different anneal temperatures were significantly different indicating again, as shown in Figure 3-1, the possibility of surface conversion.

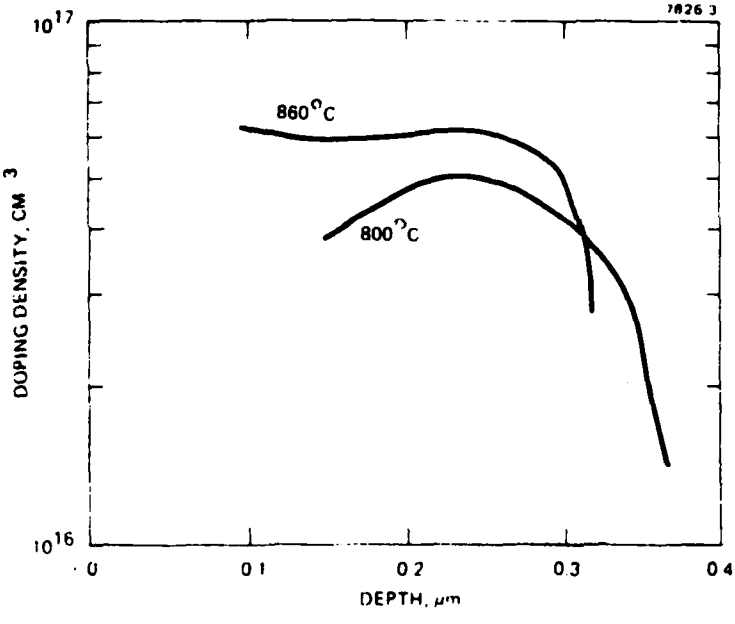


Figure 3-1.
Doping density versus depth for two different annealing temperatures.

From these experiments it can be concluded that the substrate has the greatest impact on the profile obtained and that the results are independent of the ion source as expected. It is also clear that the maximum usable anneal temperature should be employed since the mobilities obtained are lower by 20 to 25% than could be expected with epitaxial material.

The nominal TELD profile is flat in doping from the surface to the maximum depth, at which point the doping drops abruptly to the background level in the semi-insulating substrate. To approximate this doping distribution with ion implantation requires multiple implants. Therefore we designed a three energy implant and tested it at two different dose levels as shown in Figures 3-2 and 3-3. These results indicate that the desired TELD profiles can be produced by multiple energy ion implantation.

Devices were fabricated on HRL-grown LPE GaAs and on VPE GaAs with buffer layers. The LPE was 2 μm thick, grown on semi-insulating GaAs with a doping density of 2.9×10^{16} cm^{-3}; the VPE had similar doping density and channel thickness but was grown on a buffer layer. Problems with depositing a 1-μm gate over a 2-μm-high mesa existed because of the thinning of the photo-resist at the edge of the mesa. Even though 1 μm of photoresist has been used to cover the wafer, the photo-resist at the edge of the mesa was less than 0.5 μm thick. When a 1-μm-long, 0.5-μm-high gate is deposited, the gate metal is not well defined over the mesa edge and will often break when the photoresist is removed. In addition, it is difficult, due to interference effects, to define a 1-μm gate with contact photolithography both on top of the mesa and on the substrate. Therefore wafers were

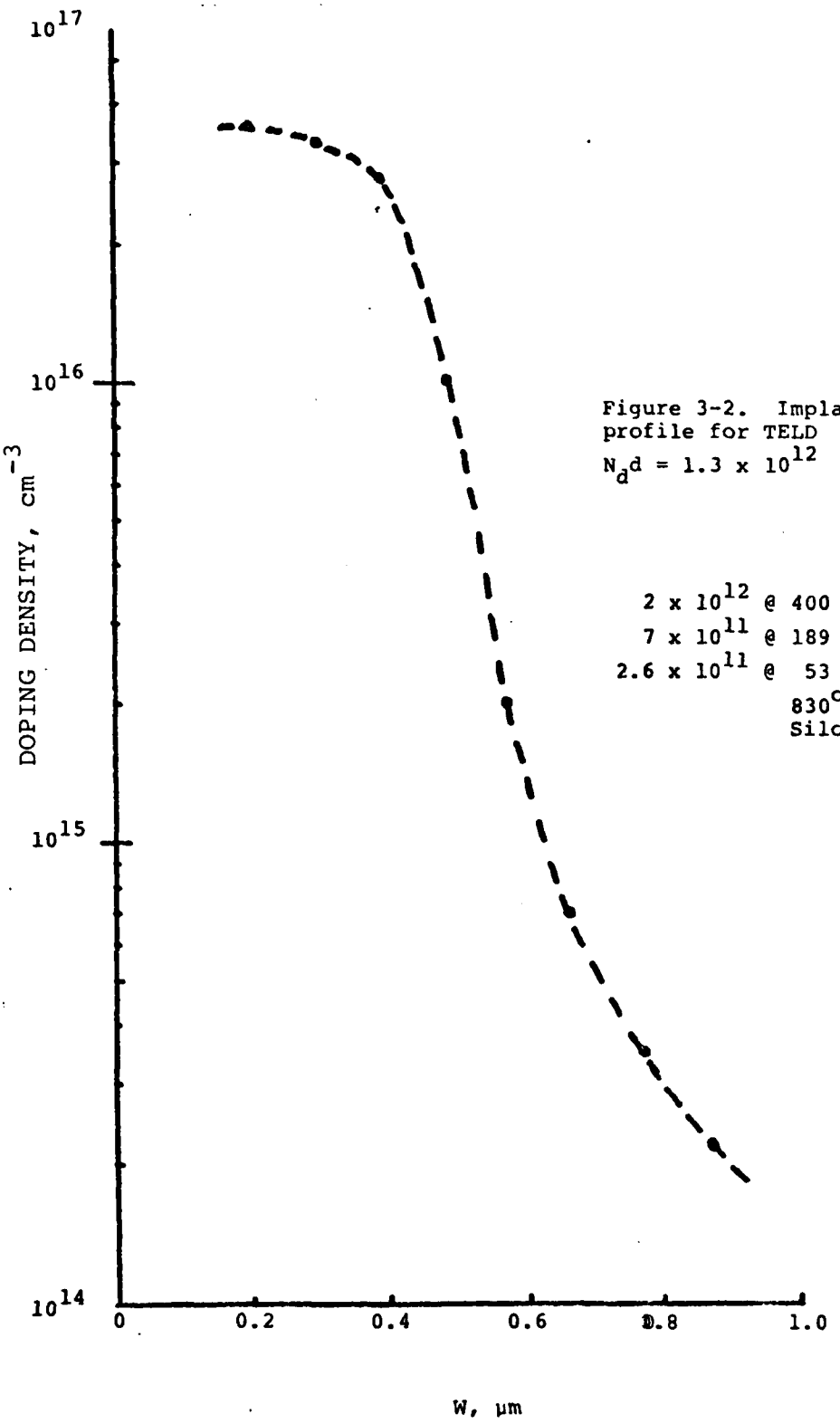


Figure 3-2. Implanted profile for TELD
$N_d d = 1.3 \times 10^{12}$

2×10^{12} @ 400 keV
7×10^{11} @ 189
2.6×10^{11} @ 53
830°C Anneal
Silox Cap

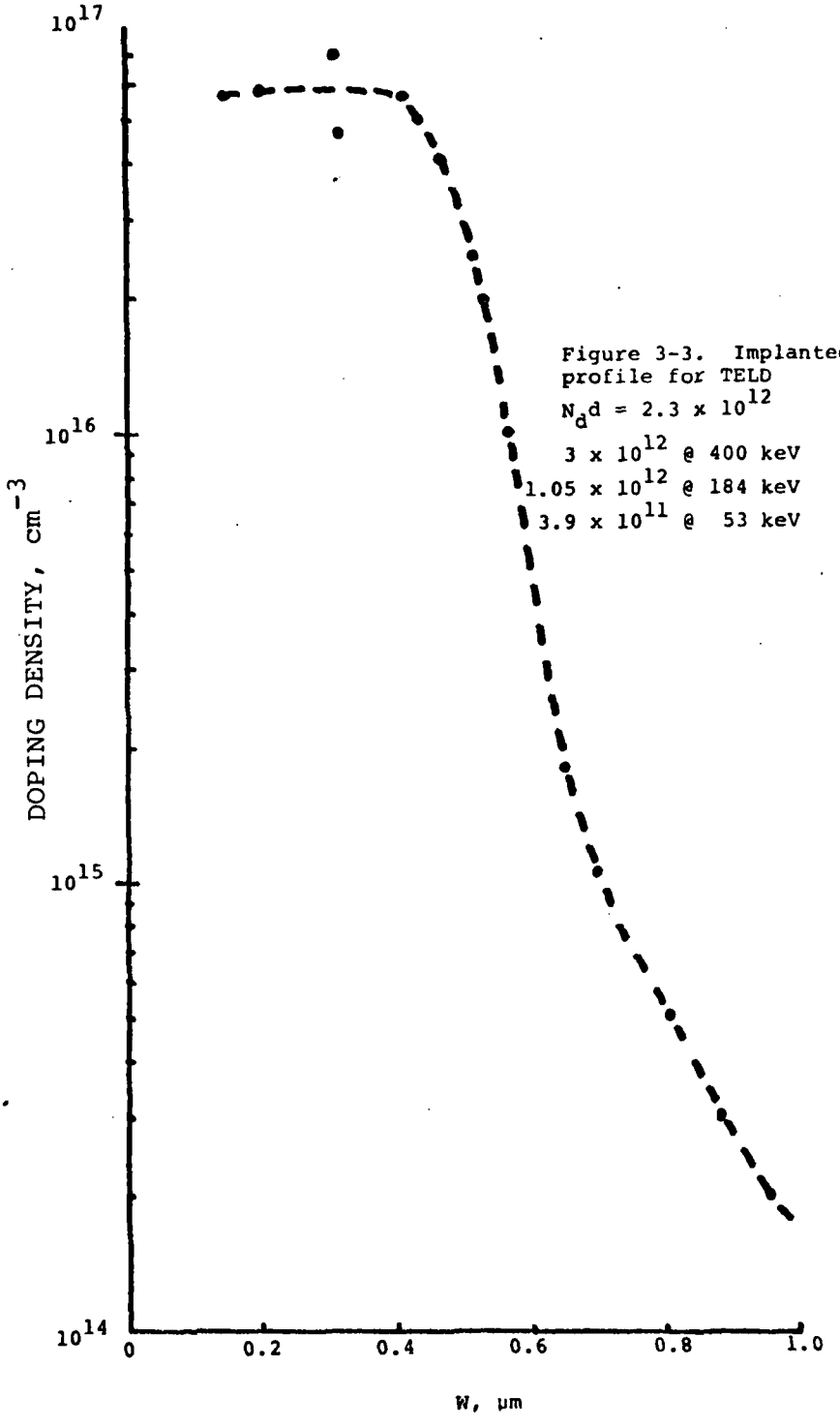


Figure 3-3. Implanted profile for TELD

$N_d d = 2.3 \times 10^{12}$

3×10^{12} @ 400 keV

1.05×10^{12} @ 184 keV

3.9×10^{11} @ 53 keV

processed with 2-μm-high mesas and gates defined by E-beam lithography. In Figure 3-4, the metal gate, which is 7500 Å long and 4000 Å thick, is shown to have excellent continuity over the 2-μm-high mesa.

Gallium arsenide anodic oxide has been grown at HRL with both aqueous and nonaqueous liquid electrolytes. Oxide grown with solutions of inorganic salts in organic solvents has been found superior to oxide grown with aqueous solutions. In particular, nonaqueous electrolytes appear generally to yield oxide/GaAs interface properties that are less sensitive to atmospheric humidity. Consequently, subject to compatibility with other process requirements, nonaqueous electrolytes will be used for oxide growth.

Incorporating anodic oxide MIS structures as GaAs IC elements presents some unique fabrication problems. Oxide must be grown on device mesas that are electrically isolated on high-resistivity substrates. Substrate resistance essentially prevents oxide growth unless, as a minimum requirement, the wafer is illuminated to excite photoconductivity. Growth is still extremely nonuniform if only edge contact is made to the wafer. Growth of a uniform oxide requires a large-area contact to the back of the wafer. The voltage drop through the substrate is then sufficiently low to ensure a uniform oxide. A proprietary, nondestructive technique for supplying the necessary back contact has been developed at HRL. In combination with illumination, this technique has been demonstrated to permit rapid growth of anodic oxide on high-resistivity material and a very uniform oxide over a region that confirms to the area of the back contact.

The intrinsic chemical vulnerability and thermal instability of the oxide place constraints on device design and fabrication.

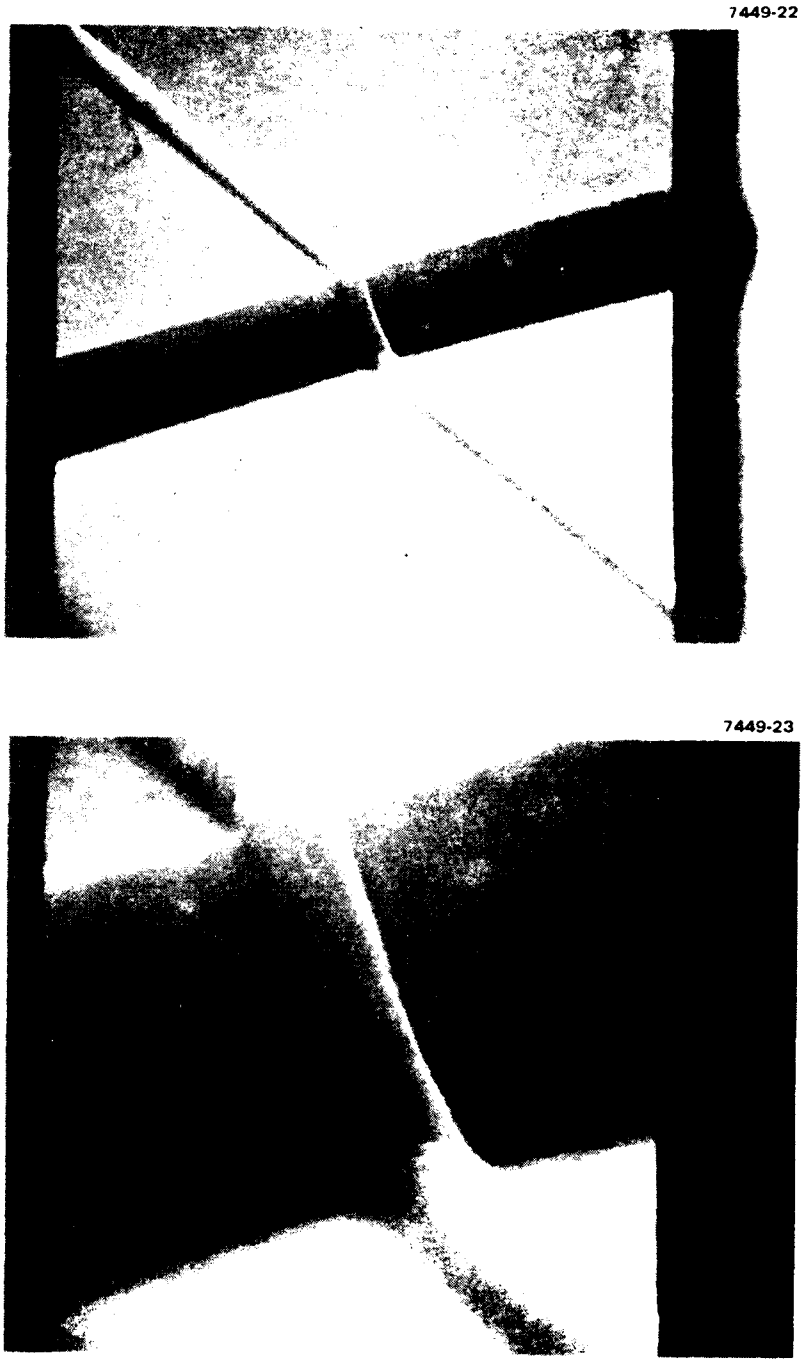


Figure 3-4 SEM photographs of 2-μm-high mesa with 7500-Å-long by 4000-Å-high gate deposited by E-beam lithography.

Anodic oxide is readily soluble in even moderately strong acids and bases. In particular, the oxide rapidly dissolves in the alkaline developer for conventional positive photoresist. As a result, the oxide is damaged by the photolithographic processing necessary to pattern the overlaying metalization. Patterning the oxide by etching is also difficult since (1) resist development and oxide etching occur with the same chemical treatment, and (2) the oxide etch rate is so high that undercutting is difficult to control.

An alternative fabrication technique that appears quite feasible is to use a single photoresist step to both control selective oxide growth and pattern the overlaying metal by lift-off. We have observed that oxide growth can be readily restricted to openings in a coating of positive photoresist. The extent of lateral growth depends on the post-development bake treatment of the resist and anodic growth parameters. Lateral growth can be limited to less than 1 μm for an oxide thickness of 0.1 μm. Following oxide growth, the desired metal layer is deposited and patterned by dissolving the photoresist with organic solvents. The solvents used do not attach the anodic oxide. Clearly, this technique requires a device design in which both the oxide and the overlaying metal have the same pattern. Direct contact of the metal to the GaAs is prevented by the lateral growth of the oxide. We expect that a nonanodizing metal lying on the high-resistivity substrate can also be exposed during anodization without significantly affecting oxide growth on the mesas.

The completed anodic oxide MIS structure remains vulnerable to chemical attack and thermal degradation, and the fabrication process must be designed to accommodate this vulnerability. If further chemical processing is essential, the MIS elements are best encapsu-

lated with a deposited, impervious dielectric. Subsequent processing temperatures are limited to about 350°C by the onset of anodic oxide decomposition, which results in the loss of As and the crystallization of the remaining Ga_2O_3. Interface properties degrade with the onset of crystallization.

IV. TELD/FET DEVICES AND CIRCUITS

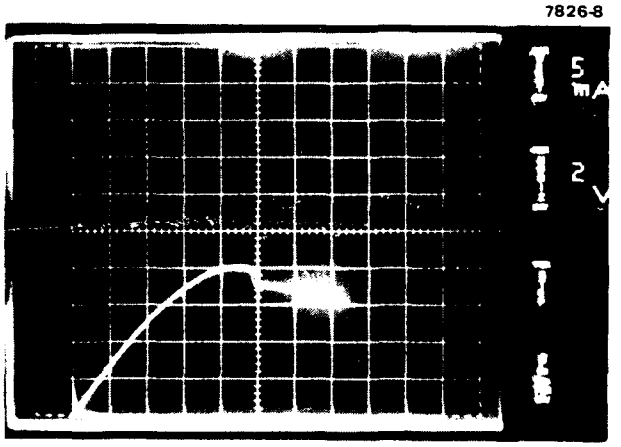
A. Introduction

Incorporating the TELD design and fabrication procedure as discussed in the previous two sections, two mask sets containing TELDs and TELD/FET circuits were designed, wafers processed and devices and circuits evaluated. The current drop, an important performance measure of TELDs, on the initial wafers processed with the first mask set was between 20% and 30%, whereas the devices on the TELD/FET circuit mask set exhibited less than 10% current drop and in most cases had no current drop. This section discusses the devices and circuits contained on the two mask sets and the experimental results obtained.

B. I-V Characteristics of TELDs.

Epitaxial wafers with an active region doping density of 2.9 x 10^{16} cm^{-3} and a thickness of 2 μm were used for fabrication of TELDs. Typical I-V characteristics for the gateless devices are shown in Figure 4-1. Table 4-1 lists the threshold current (V = 10V), the current above threshold (V = 14V), and the percentage current drop for the devices tested. The average current drop was 25.3% for the two terminal devices.

In order to define short gates over the high (3 μm) TELD mesas, E-beam lithography was used because of its depth of field capabilities. SEM microphotographs of a single and dual-gate TELD are shown in Figure 4-2 and 4-3. The I-V characteristics of two adjacent TELDs are shown in Figure 4-4, one without and one with a 0.5 μm long gate. The threshold conditions for the two devices were 20 mA at 9.4 V and 18.4 mA at 8.4 V, respectively. The effect of the gate bias on the threshold conditions as shown in the figure are listed in Table 4-2. The I-V characteristics for the dual-gate TELD are shown in Figure



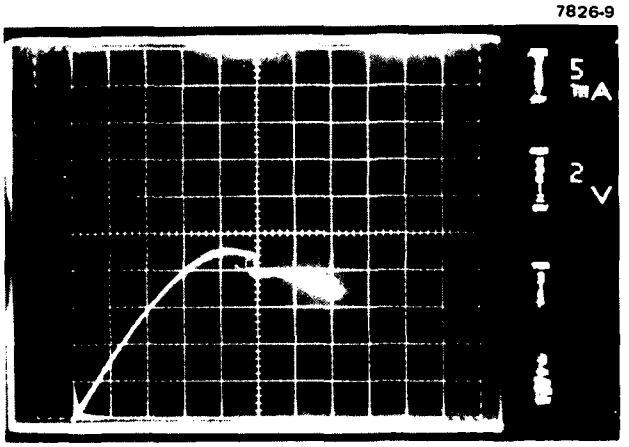
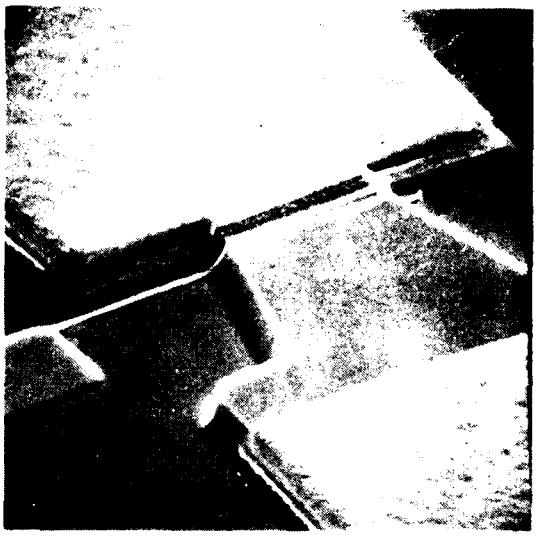
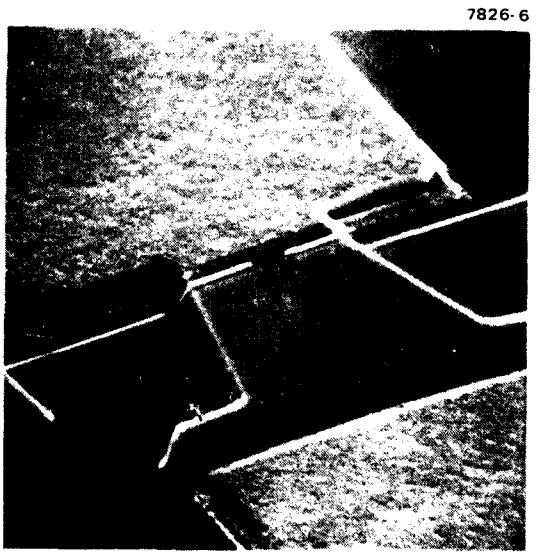


Figure 4-1. Typical I-V characteristics for gateless TELD



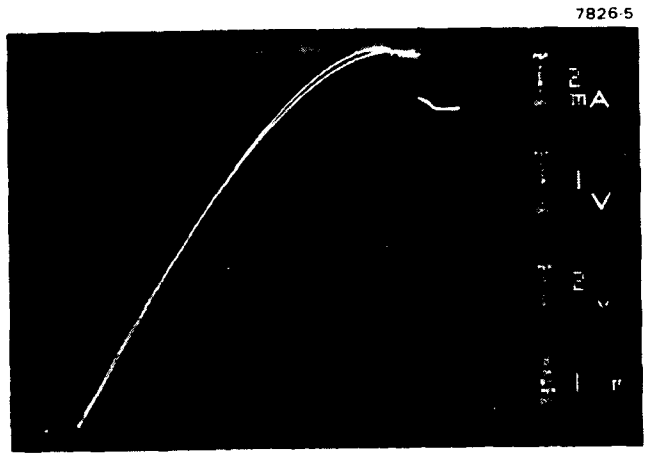
(a) SINGLE GATE

Figure 4-2. SEM microphotography of single gate TELD

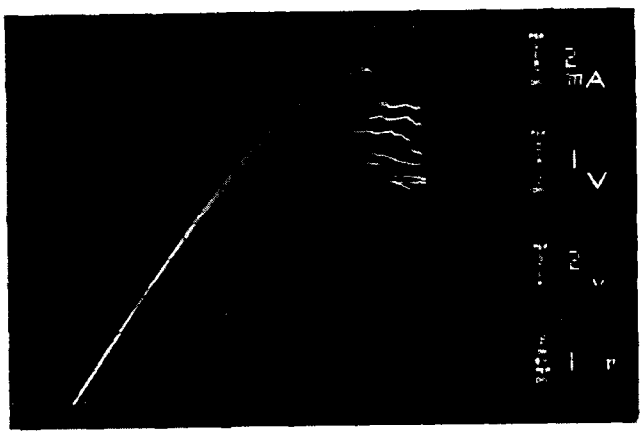


(b) DUAL GATE

Figure 4-3. SEM microphotograph of dual-gate TELD



(a) TWO TERMINAL



(b) THREE TERMINAL

Figure 4-4. I-V characteristics of two-and three-terminal TELDs.

4-5 for two different gate bias conditions.

Table 4-1. "Drop Back" Characteristics of TELDs

Device No.	Threshold Voltage volts	Threshold Current (V=10V) mA	Above Threshold Current (V=14V) mA	% Drop K
1	8	21	17	19
2	8	21	15	29
3	8	23.5	19	19
4	8	24	20	17
5	8	23	17	26
6	8	22.5	17	24
7	8	23	17	26
8	8	24.5	18	27
9	8	23	17	26
10	8	24.5	18	27
11	8	23	17.5	24
12	9	20	15.5	23
13	9	19	14.5	24
14	9	18	13	28
15	9	18	13	28
16	9	18	13	28
17	9	18	13	28
18	9	17.5	12.5	29
19	9	18	13	28

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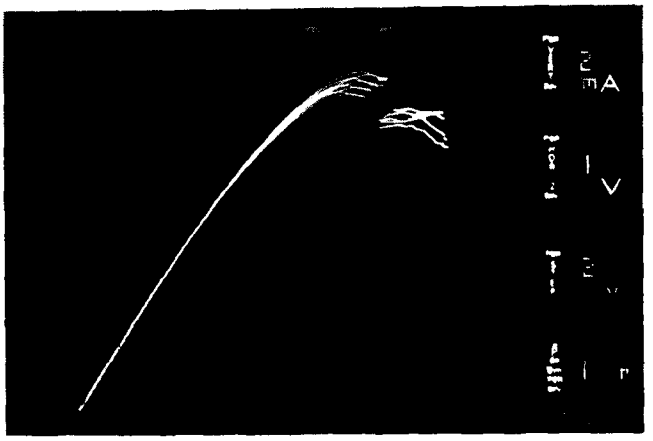
(a)

V_{g2} = 0 V, V_{g1} = 0, −2, −4, −6, −8



(b)

V_{g2} = −4, V_{g1} = 0, −2, −4, −6, −8

Figure 4-5. I-V characteristics of dual-gate TELD.

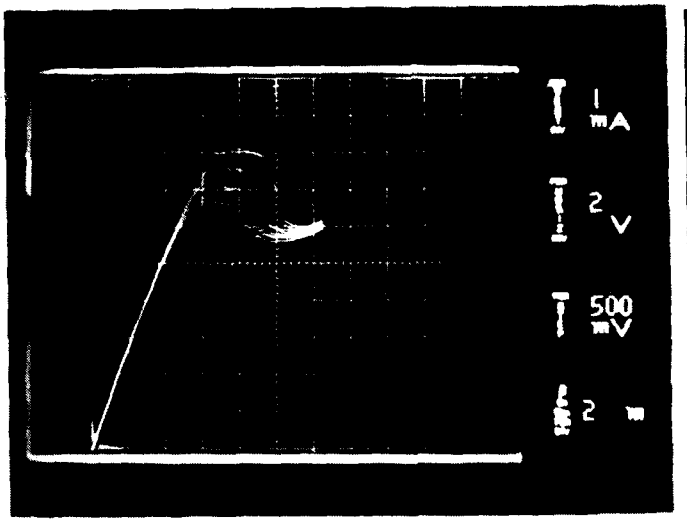
Table 4-2. TELD Threshold Conditions

V_{gc}, V	V_{AC}, V	I_{AC}^{k} mA	K %
0	8.4	18.4	13.0
-2	7.9	17.5	11.4
-4	7.5	16.5	9.0
-6	7.0	15.6	8.5
-8	6.5	14.6	7.5

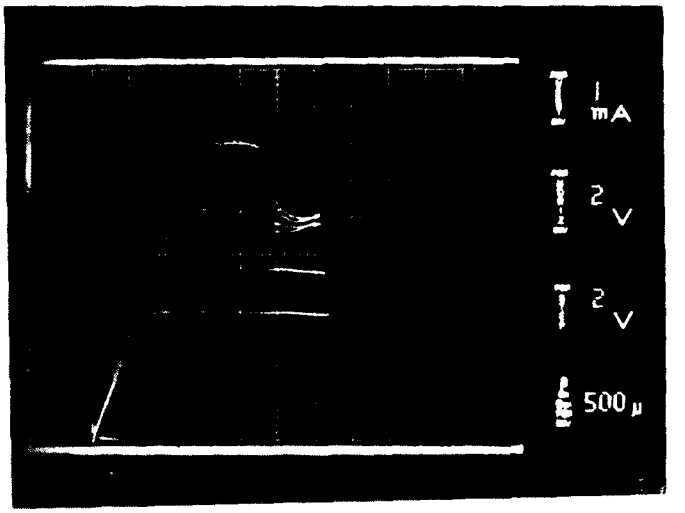
Devices were also fabricated on ion-implanted, Cr-doped semi-insulating GaAs and their I-V characteristics compared with the TELDs fabricated on epitaxial material. Typical results are shown in Figure 4-6 for a gated, ion-implanted TELD and for an epitaxial TELD fabricated in the same processing run. This comparison was made for wafers processed in the same run since, as mentioned in Section III, device repeatability from run to run was poor for our TELDs. The ion-implanted device has a much thinner active region and thus the threshold current is smaller and the current drop disappears (4-6b) for large gate bias due to the large X/d_o ratio (Section II).

C. rf Characteristics of TELDs

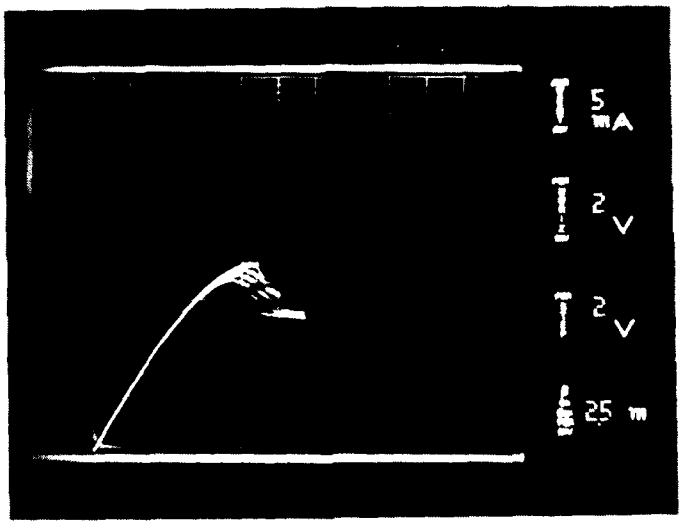
The gateless TELDs were mounted in a coplanar waveguide circuit and tested to determine their transit time frequency, 2.75 and 3.0 GHz. A typical spectrum is shown in Figure 4-7. The oscillation frequency for these devices (l_{gA} = 28 μm) was between 2.75 GHz and 3.0 GHz.



a) Ion Implanted TELD



b) Ion Implanted TELD



c) LPE TELD

Figure 4-6. I-V characteristics of TELDs.

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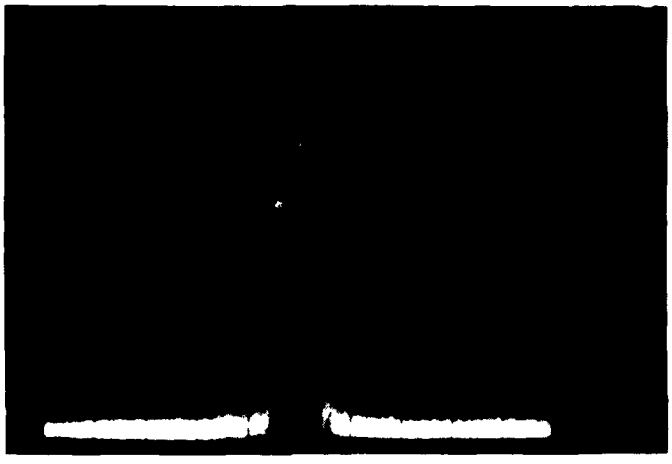

Figure 4-7.
Spectrum of TELD transit time frequency (f_o = 2.94 GHz, vertical = 10 dB/div, horizontal = 1 MHz/div, V_{bias} = 11.1 V, I_D = 14.4 mA).

In addition to the transit time frequency, the TELD could also be tuned to oscillate at a much lower frequency - approximately one-third the transit time frequency. The spectrum is shown in Figure 4-8. Both the LPE and VPE TELDs with buffer layers exhibited this low-frequency oscillation; however, it was much easier to obtain it in the LPE than in the VPE TELDs. An explanation for the low-frequency oscillation is not readily available. A possible explanation for this low-frequency oscillation is that it is the result of dielectric loading on the domain by the substrate.[12] Also the effect of the interface states between the active region and the bulk GaAs must, due to the difference between nonbuffered LPE TELDs and the buffered VPE TELDs, have some effect.

The TELDs have also been tested as frequency dividers by injecting a signal at two and three times the transit time frequency. With the devices biased slightly below threshold, we were able to trigger the device and obtain output at one-half (in the first case) or one-third (in the second case) the input signal. For the divide-by-two circuit, an instantaneous bandwidth at the input frequency of 80 MHz was obtained, and the TELD could be tuned to divide by two from 5.2 GHz to 5.6 GHz. The output spectrum for the divide-by-two case is shown in Figure 4-9. Trigger sensitivity measurements were not made. The threshold voltage was 10.4 V at just over 17 mA, and, with an input signal amplitude of just under 1 V, the device was triggered and divided the input signal by two. For the divide-by-three circuit, the input frequency was 8.25 GHz, and the instantaneous bandwidth at the input frequency was 30 MHz. For this setup, the circuit also divided by nine, resulting in an output frequency of 0.917 GHz (transit time frequency = 2.75 GHz). For this case, all

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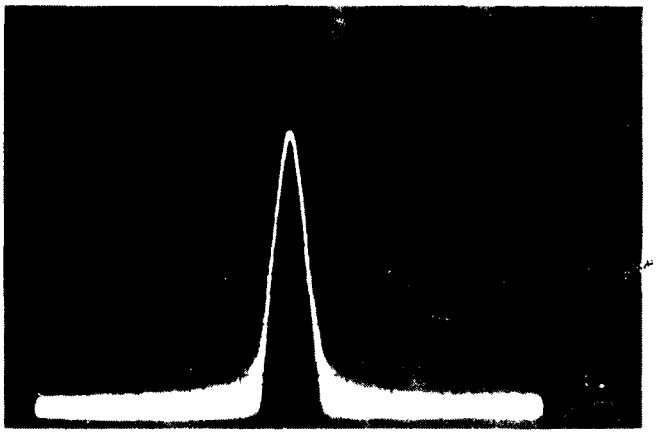

Figure 4-8.
Spectrum of TELD low-frequency oscillation (f_o = 1.001 GHz, vertical = 10 dB/div, horizontal = 500 kHz/div, V_{bias} = 11.1 V, I_D = 14.5 mA).

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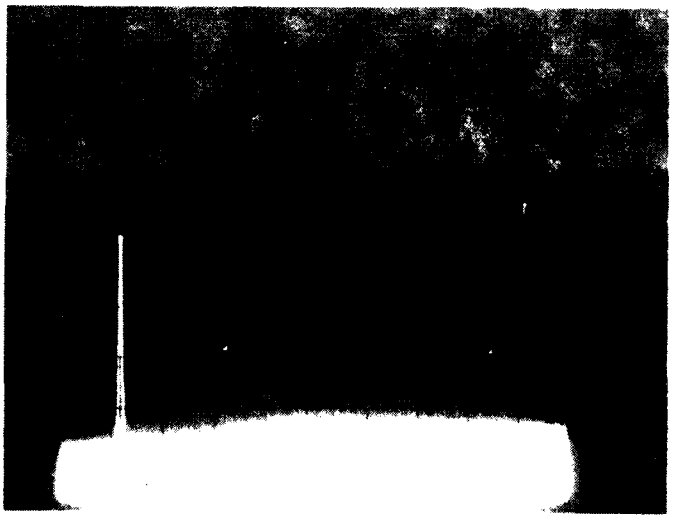


Figure 4-9.
Output spectrum for divide-by-two TELD (2.720 $\leq f_o \leq$ 2.769 GHz, V_{bias} = 10.13 V, I_D = 17 mA).

the harmonics were present and 20 dB down from the input signal except for the transit time frequency, which was only 2 dB down in amplitude. For a similar device with a transit time frequency of 2.365 GHz, the input and output waveforms for the divide-by-three case are shown in Figure 4-10.

By retuning the circuit, the TELD divided by 2, 3, or 5 down to the low-frequency oscillation of 1.077 GHz. The input and output waveforms for the three cases are shown in Figure 4-11.

D. TELD/FET Circuits

Based on the TELD design, processing procedure and experimental results discussed previously, a mask set containing TELD/FET circuits was designed. The devices and circuits contained on the mask set are listed in Table 4-3. The circuits were fabricated on epitaxial material designed for optimizing the TELD performance. The TELDs were fabricated by etching mesas in the epitaxial GaAs and the FETs by selectively ion implanting into the semi-insulating GaAs. A combination of photo and E-beam lithography was used to define the different gates.

A CALMA plot and a photograph of the entire chip are shown in Figure 4-12. The chip is approximately 140 mils on a side and is divided into four quadrants. The first quadrant contains several TELD/FET circuits including a BPSK modulator. The second quadrant has TELD frequency dividers, both single and dual gate, the processing test patterns, and a MIM capacitor. TELD/FET circuits including a 13-stage ring oscillator are contained in the third and fourth quadrant of the chip. The small crosses on the chip are used for registration of the E-beam machine when defining 0.5 μm long gates. Figure 4-13 through 4-17 show several different TELD/FET frequency divider circuits. Discrete devices for frequency division with an output of 1 GHz and 5 GHz are shown in Figure 4-13. Due to

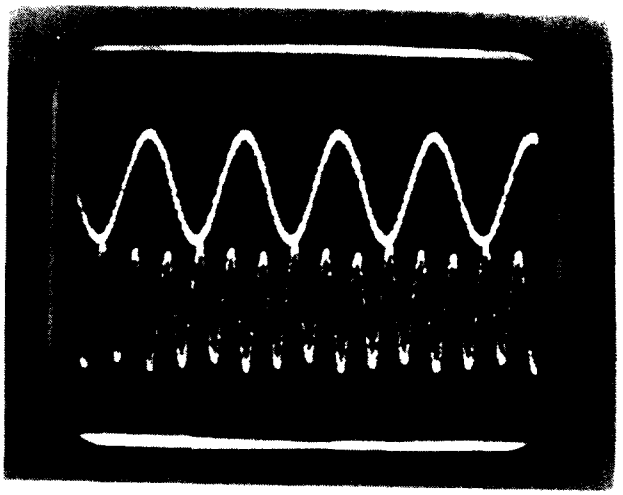


Figure 4-10. Divide-by-three TELD (f_{in} = 7.095 GHz, f_o = 2.365 GHz).

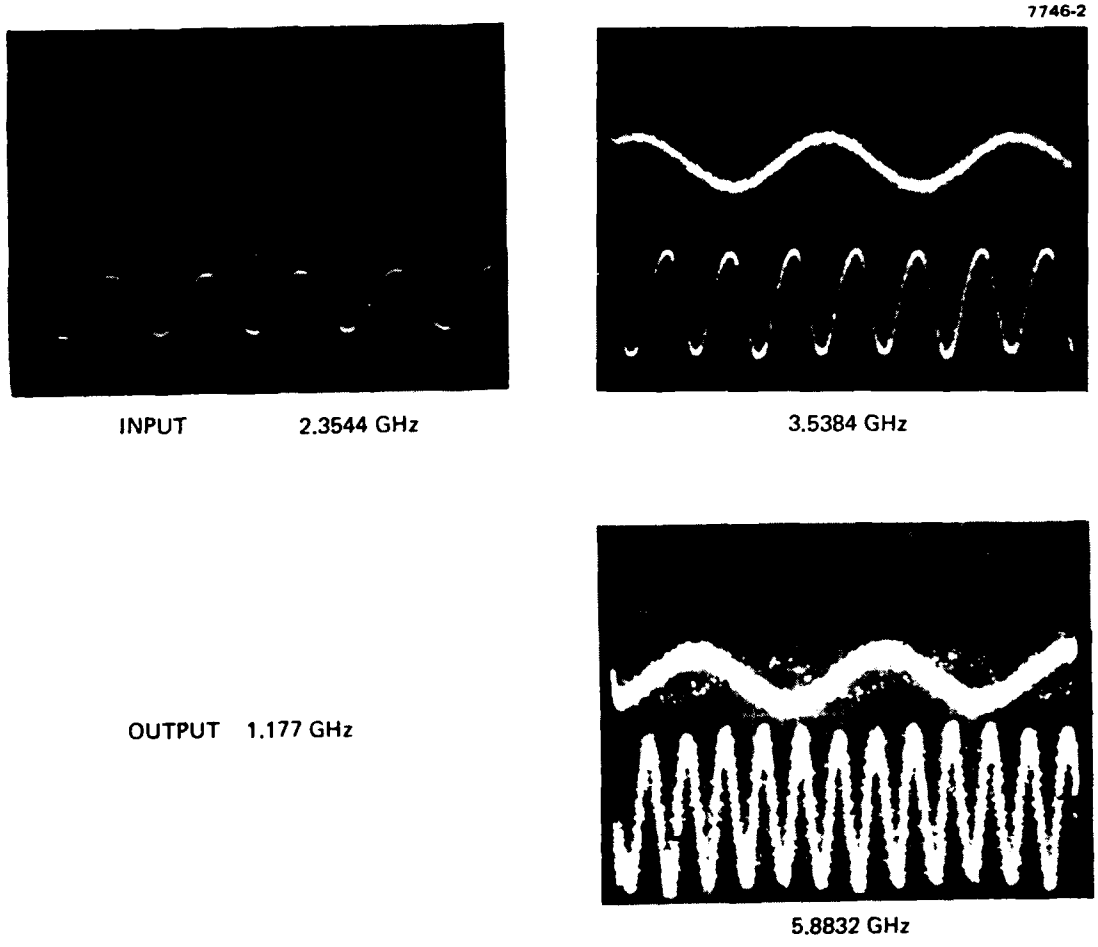


Figure 4-11. TELD frequency division.

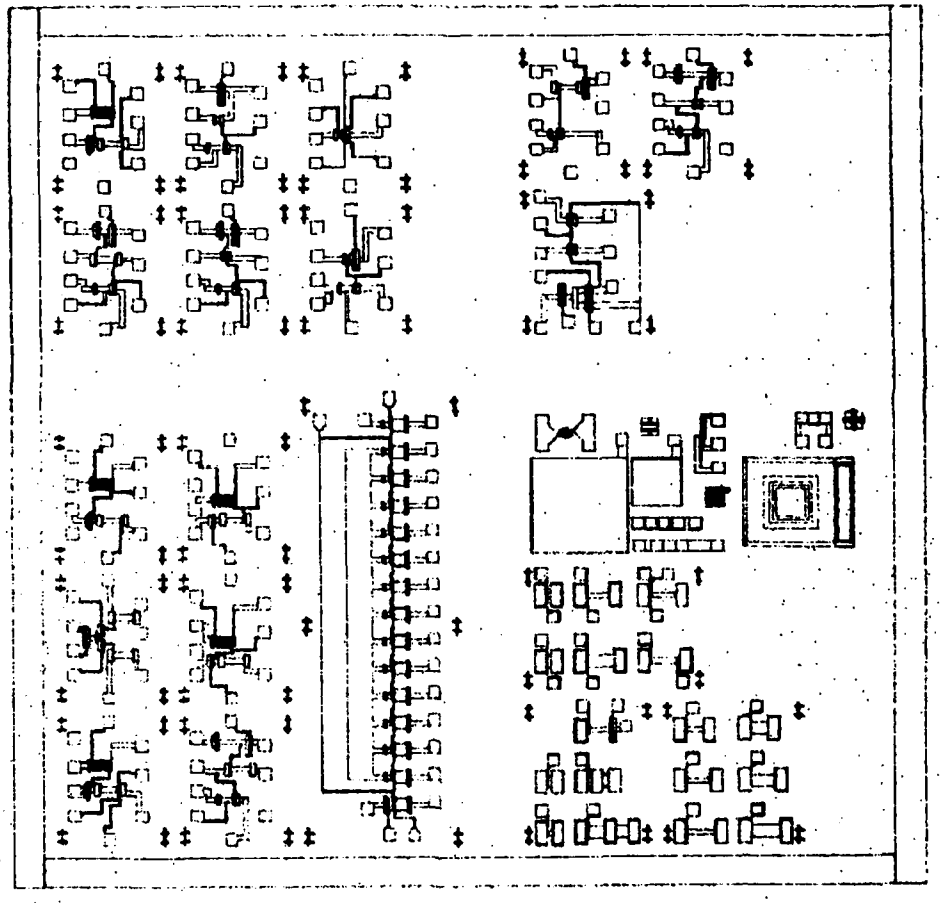


Figure 4-12 a) CALMA plot of TELD/FET circuit mask.

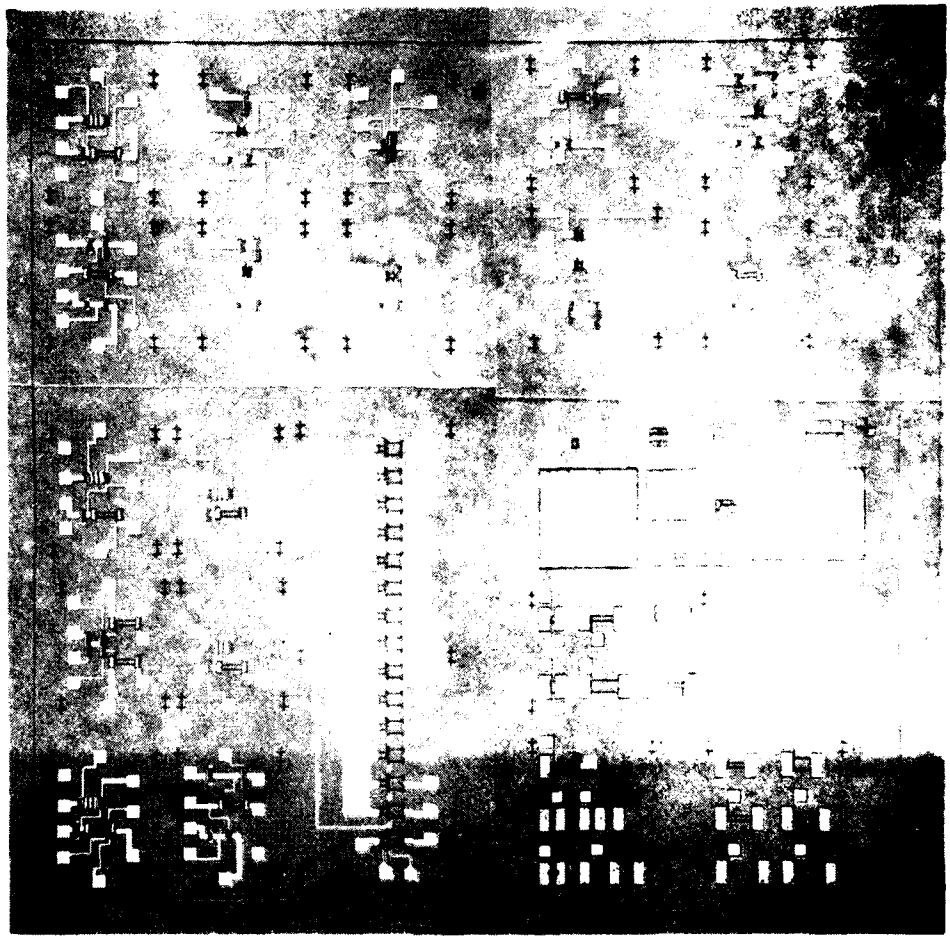
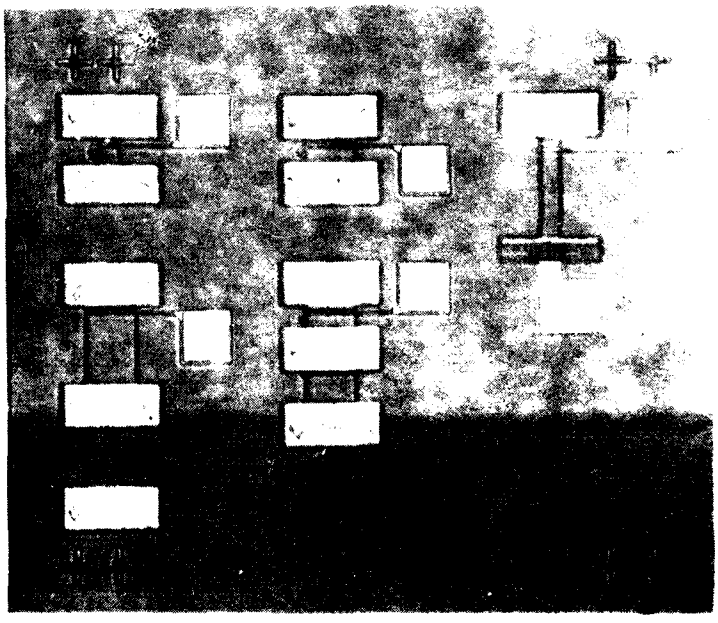


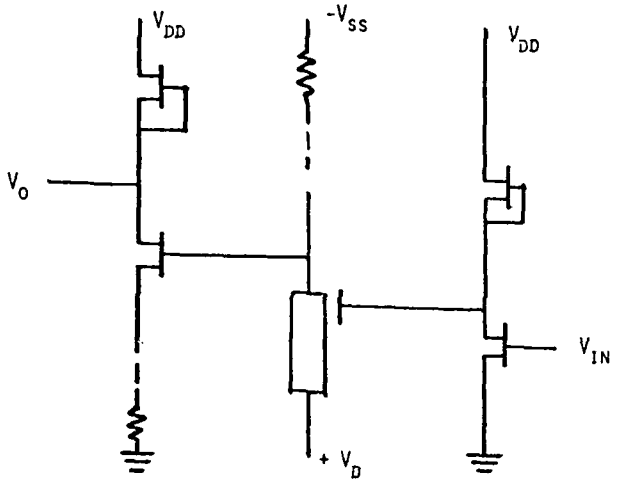
Figure 4-12 b) Picture of fabricated chip of TELD/FET circuit mask.

a) CALMA plot



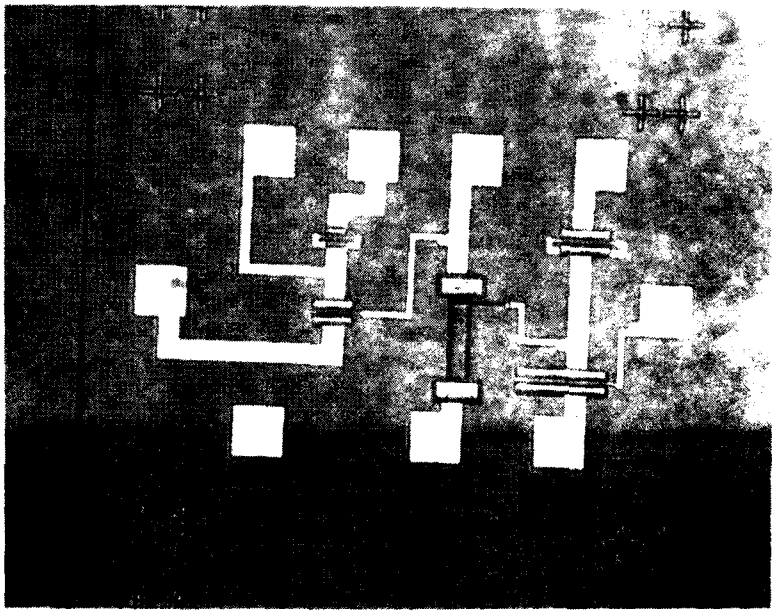
b) Fabricated circuits

Figure 4-13. TELD frequency dividers (f_o = 1 GHz and 5 GHz).



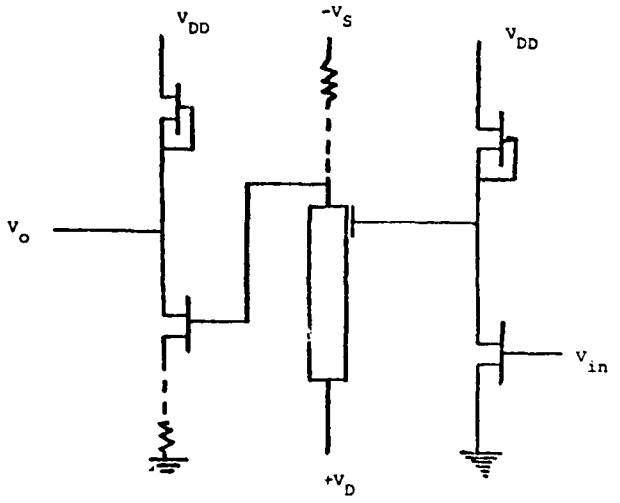
a) Equivalent circuit

b) CALMA plot

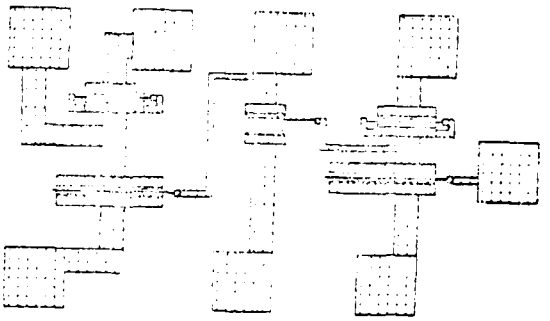


c) Fabricated circuit

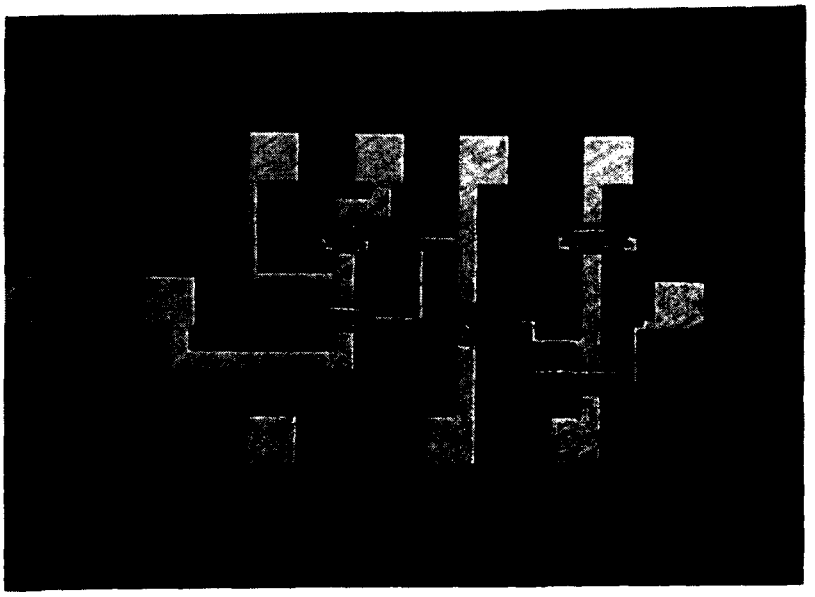
Figure 4-14. TELD frequency divider (f_o = 1 GHz)



a) Equivalent circuit

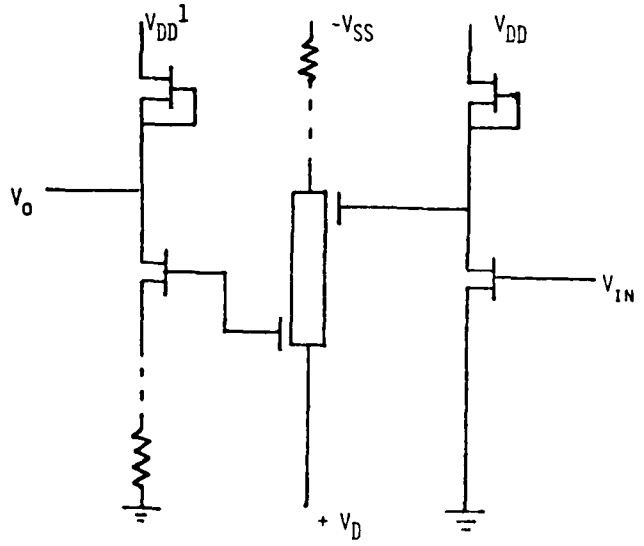


b) CALMA plot



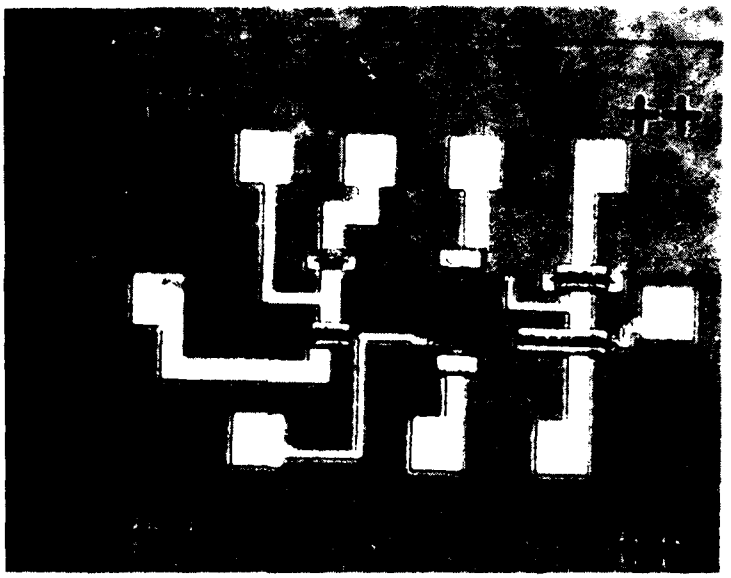
c) Fabricated circuit

Figure 4-15. TELD frequency divider (f_o = 5 GHz).



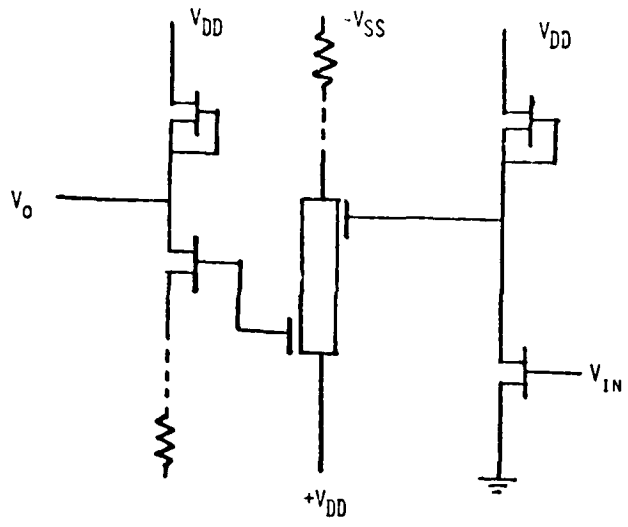
a) Equivalent circuit

b) CALMA plot



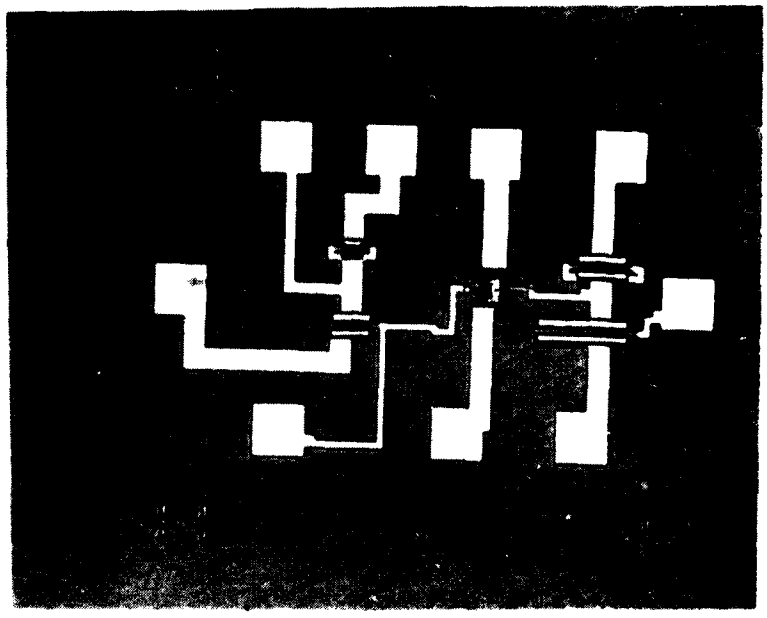
c) Fabricated circuit

Figure 4-16. TELD/FET frequency divider with capacitive pickoff (f_o = 1 GHz).



a) Equivalent circuit

b) CALMA plot



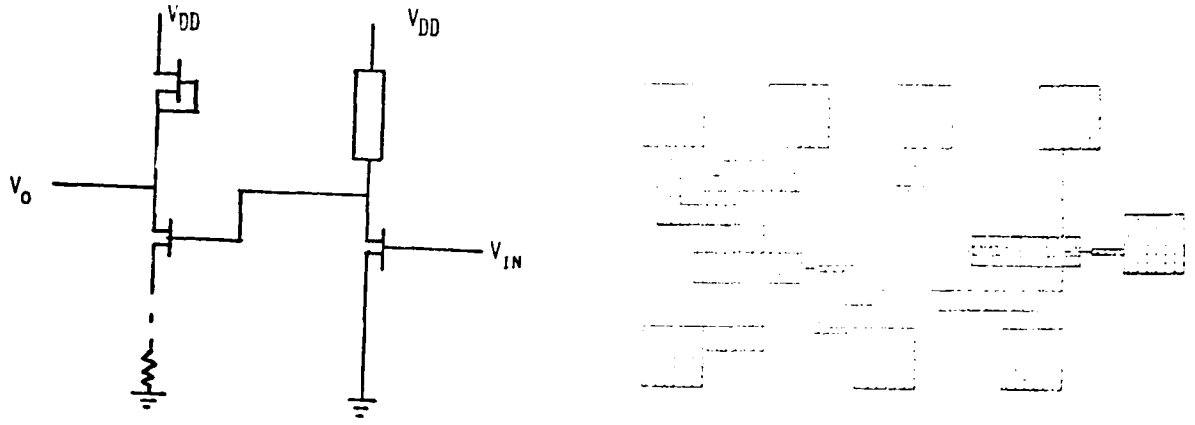
c) Fabricated circuit

Figure 4-17. TELD/FET frequency divider with capacitive pickoff (f_o = 5 GHz).

the variations in mobility between different epi and ion implanted material for TELDs, frequency dividers with gate-to-anode spacing of 70, 100 and 120 μm were fabricated. In order to investigate the fanout capability or the ability of the TELD output to go "off chip", TELDs with 20 μm and 50 μm widths were used. Figure 4-14 and 4-15 show TELD/FET frequency divider circuits with 1 GHz and 5 GHz fundamental frequencies. Both the input and output FETs have 0.5 μm gate length FET for the 5 GHz circuit. Figure 4-16 shows a similar circuit, however, with a capacitive pick-off probe on the TELD. Finally, Figure 4-17 is the same as 4-16 except that the fundamental frequency of the TELD is 5 GHz rather than 1 GHz. All of these circuits require "off chip" resistors and separate bias supplies for proper operation.

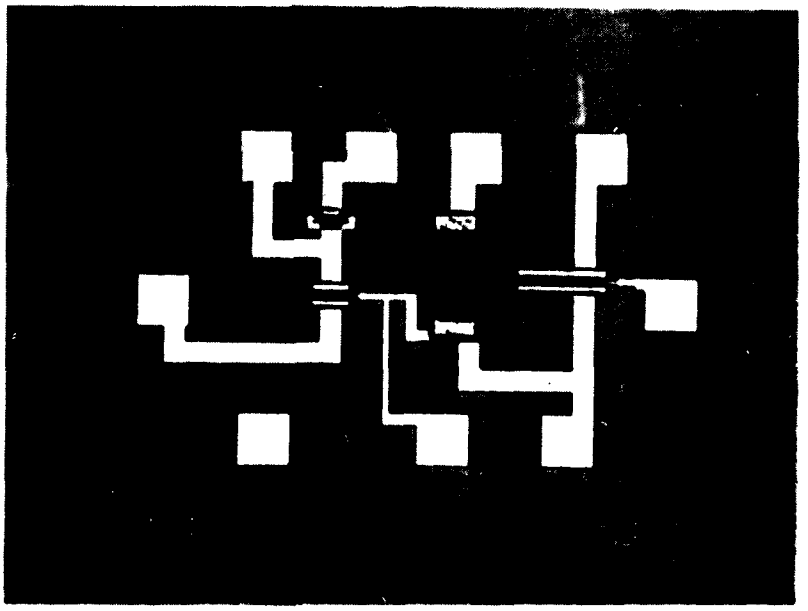
Figure 4-18 through 4-21 show TELD/FET circuits in which the TELD is triggered with an FET. The outputs are either at the cathode of the TELD or are capacitively coupled through a pick-off probe and are buffered off chip through a FET buffer. Both 1 GHz and 5 GHz TELDs are incorporated so both 1 μm and 0.5 μm long gate FETs are used, the latter being fabricated by E-beam lithography.

Figure 4-22 and 4-23 show two inverter circuits in which the TELDs is triggered with an FET and the output is level shifted through an FET source-follower and three Schottky-barrier diodes. Figure 4-24 and 4-25 are also inverter circuits incorporating dual- and triple-gate TELDs with an FET load. Figure 4-26 is a TELD/FET, exclusive OR circuit using two, dual-gate FETs with 0.5 μm long gates and a capacitively coupled, 5 GHz TELD. A 13 stage ring oscillator is shown in Figure 4-27 incorporating a TELD input to trigger the oscillator and output stage with capacitively coupled output.



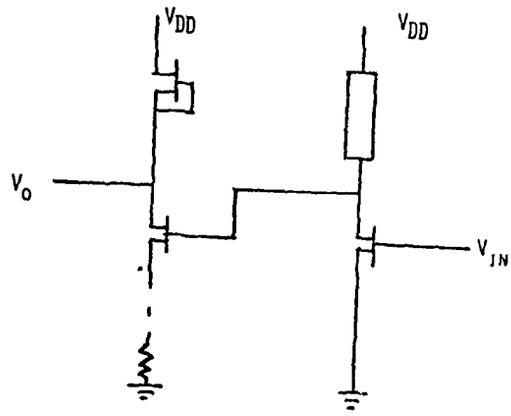
a) Equivalent circuit

b) CALMA plot



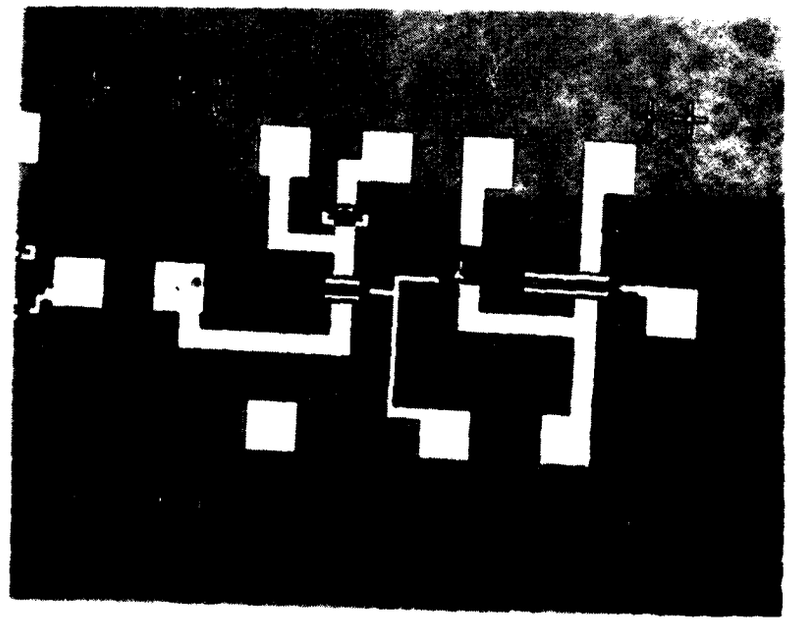
c) Fabricated circuit

Figure 4-18. 1 GHz TELD with FET switch



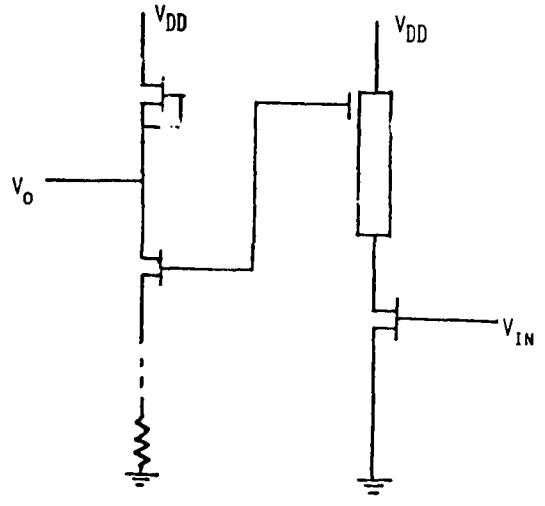
a) Equivalent circuit

b) CALMA plot

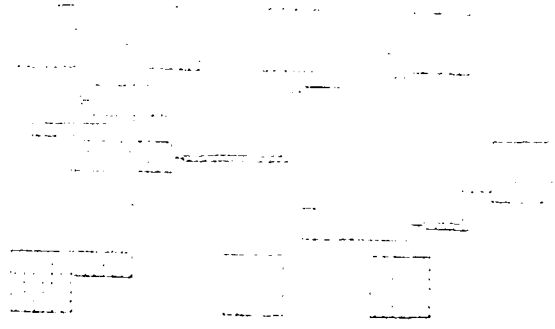


c) Fabricated circuit

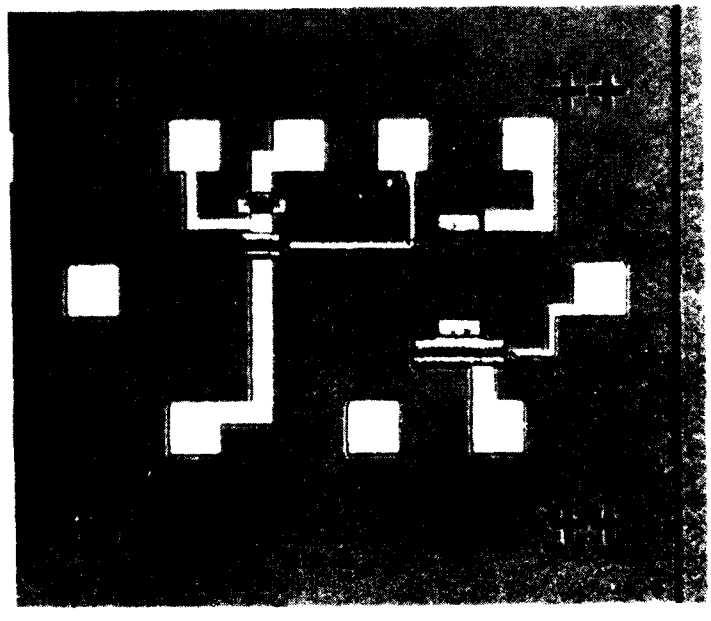
Figure 4-19. 5 GHz TELD with FET switch.



a) Equivalent circuit

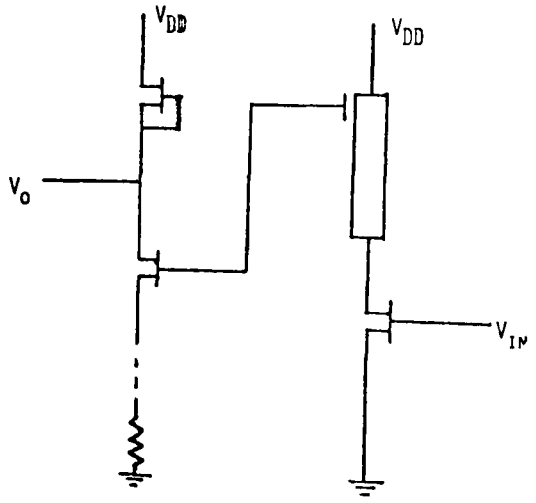


b) CALMA plot



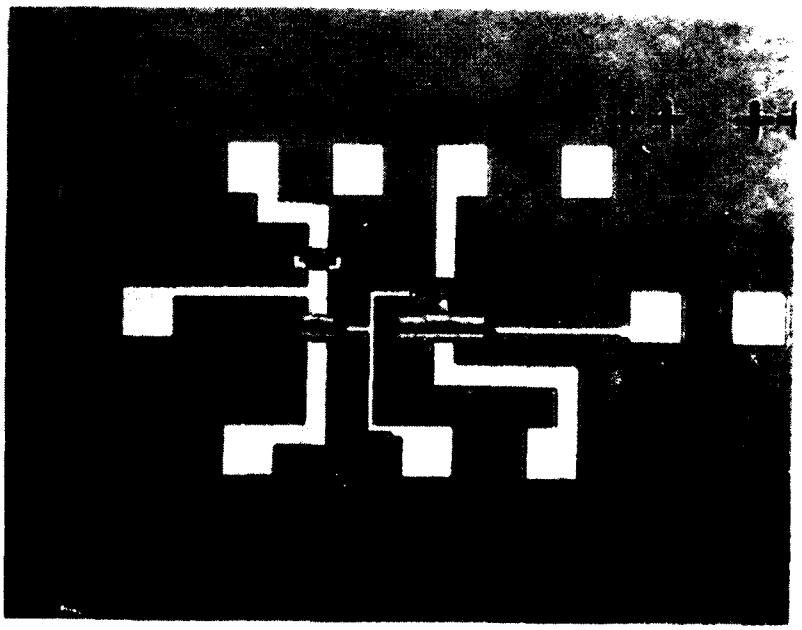
c) Fabricated circuit

Figure 4-20. 1 GHz, capacitive pickoff TELD with FET switch.



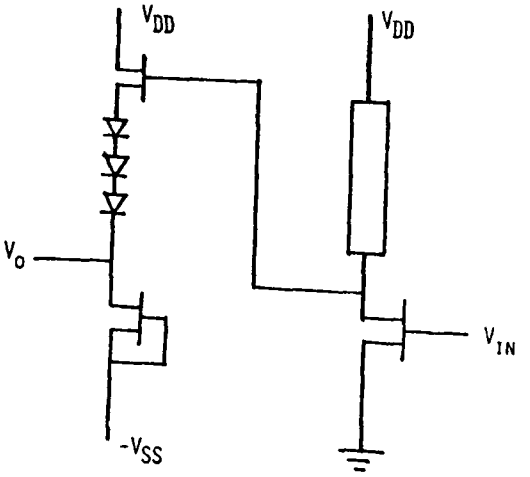
a) Equivalent circuit

b) CALMA plot



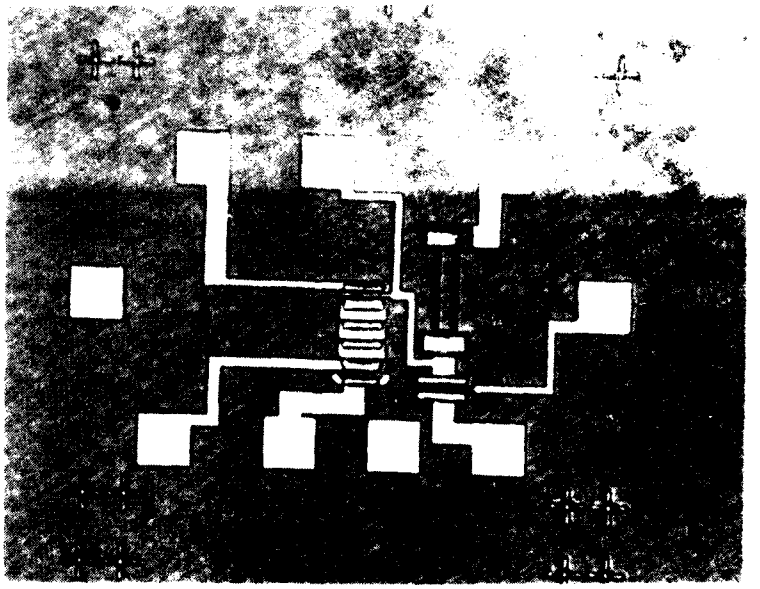
c) Fabricated circuit

Figure 4-21. 5 GHz, capacitive pickoff TELD with FET switch.



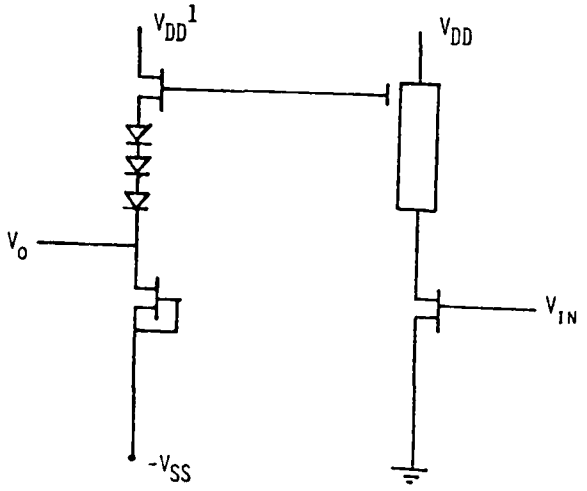
a) Equivalent circuit

b) CALMA plot



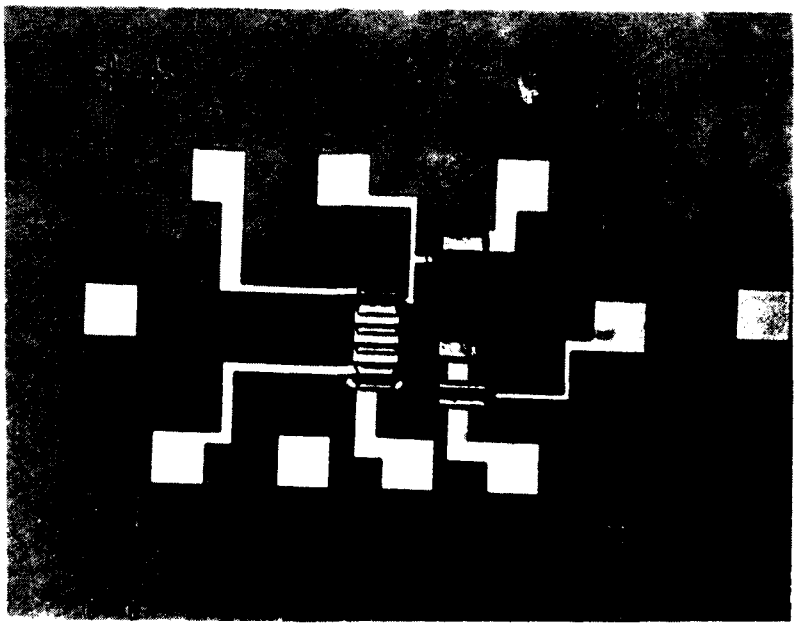
c) Fabricated circuit

Figure 4-22. TELD/FET dynamic inverter.



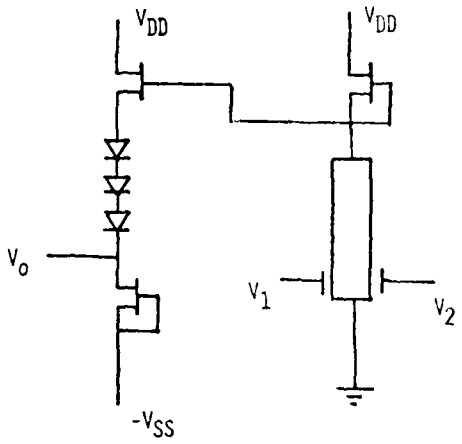
a) Equivalent circuit

b) CALMA plot



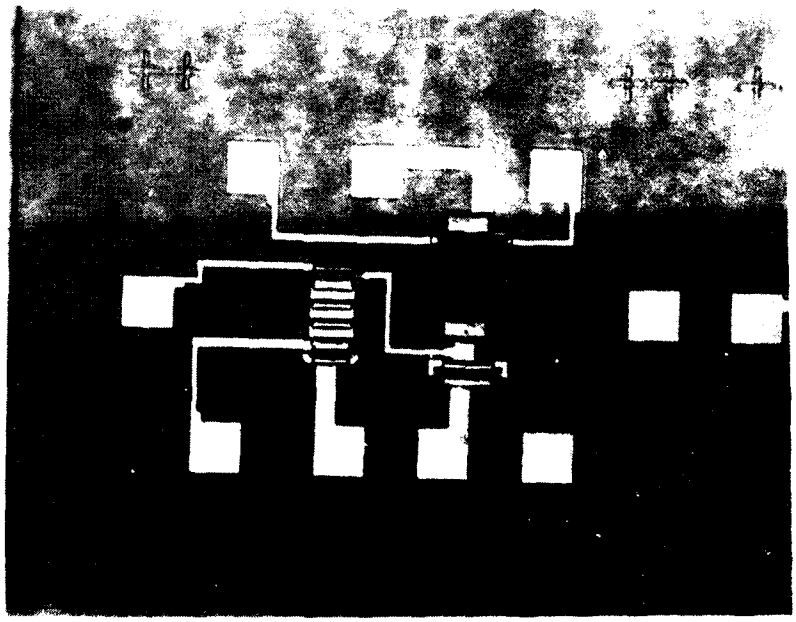
c) Fabricated circuit

Figure 4-23. TELD/FET dynamic inverter with TELD capacitive pickoff.



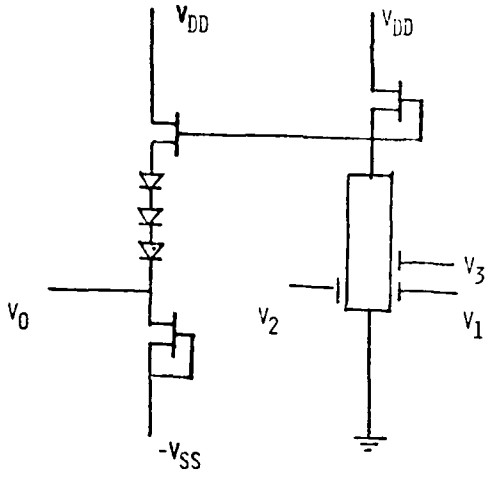
a) Equivalent circuit

b) CALMA plot



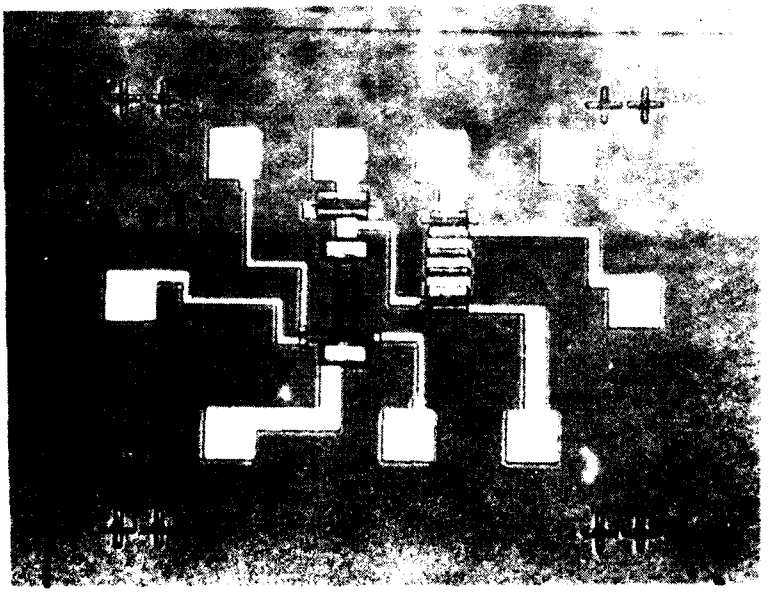
c) Fabricated circuit

Figure 4-24. Dual-gate TELD with FET load and Schottky-diode level shifters.



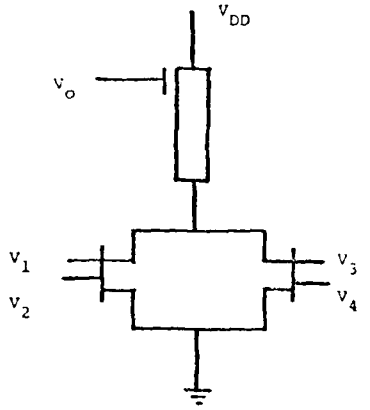
a) Equivalent circuit

b) CALMA plot



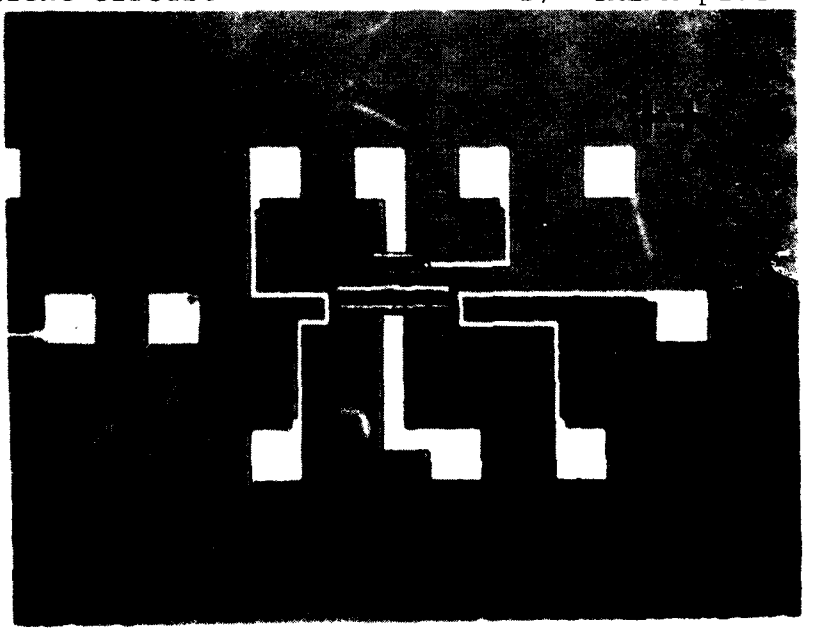
c) Fabricated circuit

Figure 4-25. Triple gate TELD with FET load and Schottky-diode level shifter.



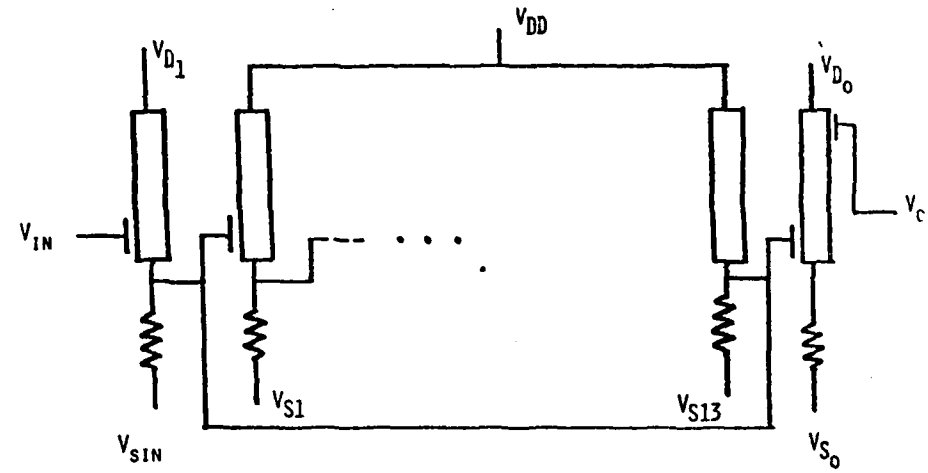
a) Equivalent circuit

b) CALMA plot

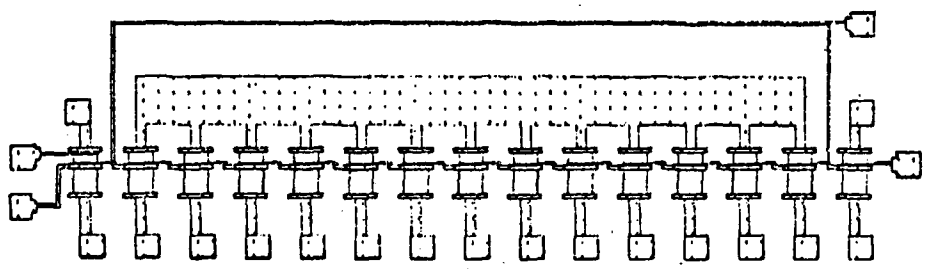


c) Fabricated circuit

Figure 4-26. Exclusive OR TELD circuit.



a) Equivalent circuit



b) CALMA plot

Figure 4-27. TELD, 13 stage ring oscillator.

Table 4-3. TELD/FET Circuits

1. Frequency Divider

   Output frequency = 1 GHz and 5 GHz

   Different gate-to-anode spacing 70 μm to 120 μm

   FET buffer output.

2. 5 GHz Modulator

3. Multi-Gate TELDs.

4. Differential Amplifier.

5. TELD Ring Oscillator

   Anode coupling between stages

6. Exclusive OR

7. TELDs with MOS pick off gates

   Anodic oxide

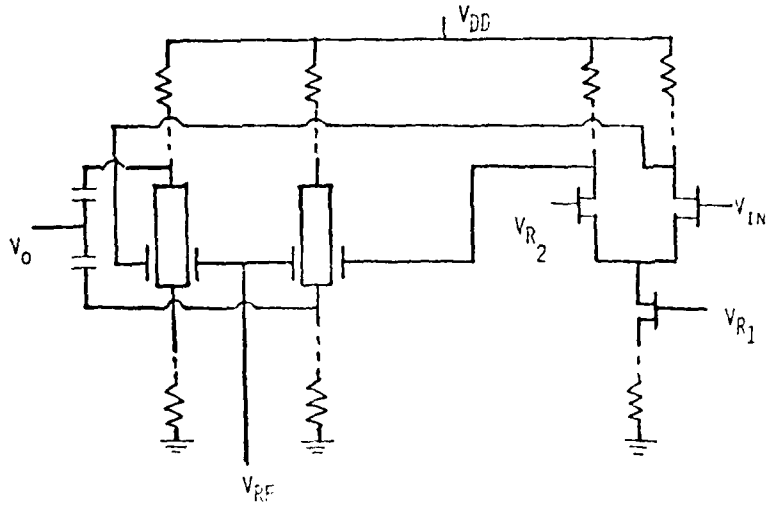
   SiO_2 glass.

8. TELD/FET combinations.

9. Material Evaluation Patterns.

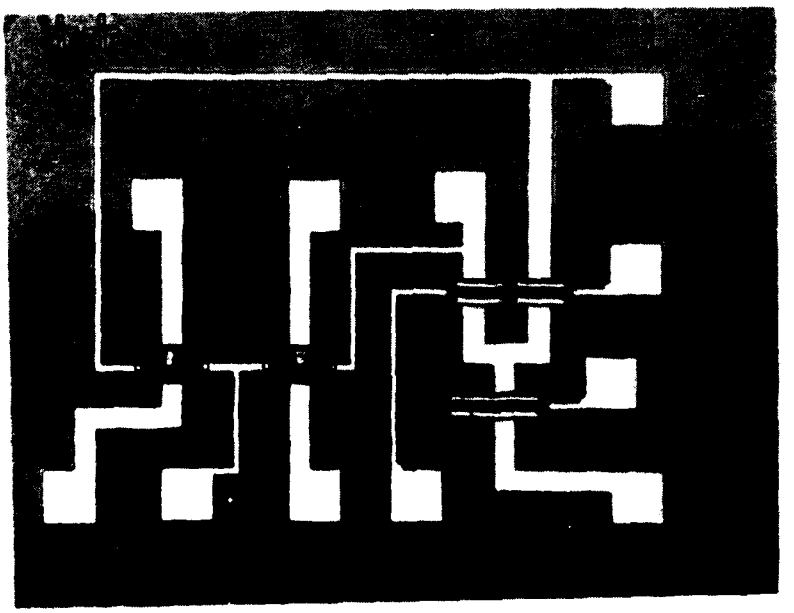
A 5 GHz modulator[13] is shown in Figure 4-28 using an FET differential amplifier on the input and two, dual-gate TELDs to provide the in phase and out-of-phase output via the cathode and anode outputs. Off chip resistors are required for proper biasing along with dc blocking capacitors in the output lines.

Processing of the TELD/FET wafers was performed as discussed in Section III, however, none of the discrete TELDs on the wafers in the two processing runs exhibited a current drop of greater than 10%. Most of the devices showed no drop at all. Operation of these circuits requires a larger current drop than was observed.



a) Equivalent circuit

b) CALMA plot



c) Fabricated circuit

Figure 4-28. TELD/FET modulator.

V. CONCLUSIONS

The objectives of this exploratory development program were to design, fabricate and evaluate TELD/FET devices and circuits. The experimental results were to be correlated with a theoretical analysis in order to determine a set of design rules for TELD/FET circuits.

A theoretical analysis for predicting the operating characteristics of the TELD was developed. The analysis was used for the design of both epi and ion-implanted GaAs TELDs. A mask set was designed for fabricating discrete TELDs in order to investigate their operating characteristics. Both dc and rf results were obtained and correlated with the analysis.

A second mask set incorporating TELD/FET circuits was designed based on the design rules obtained from the first mask set and analysis. A process schedule was developed for fabricating both TELD and FETs with 1 μm and 0.5 μm long gates on epitaxial and ion implanted GaAs wafers. Several wafers were processed, however, the current drop of the TELDs was not satisfactory for the successful operation of any of the circuits. Material reproducibility for epitaxial and ion implanted GaAs wafers was not sufficient to obtain repeatable results. Because of the relatively low doping density requirements for TELDs (1 to 5 x 10^{16} cm^{-3}), the successful fabrication of TELD/FET circuits using either ion implantation or epitaxial growth must await the development of higher quality GaAs semi-insulating substrates.

REFERENCES

1. Copeland, J.A., "Stable Space-Charge Layers in Two-Valley Semiconductors," J. Appl. Phys. 37:3602 (1966)
2. Sze, S.M., Physics of Semiconductor Devices, John Wiley & Sons, 1969.
3. Claxton, D.H., Mills, T.G., and Leisher, T.D., "Transferred Electron Device Design and Circuits," Final Technical Report, Contract F33615-75-C-1219, TRW Defense and Space Systems, Redondo Beach, California, February 1977.
4. Schlachetizki, A., and Mause, K., "Measurements of the Influence of the nd product on the Gunn Effect," Electron. Lett. 9:268 640-642, 28 December 1972.
5. Curtice, W.R., "Transverse TELDs (Transferred-Electron Logic Devices)," Annual Report, Contract N00014-76-C-0465, RCA Laboratories, Princeton, NJ
6. Mause, K., Schlachetzki, A., Hesse, B., and Salow, H., "Monolithic Integration of Gallium Arsenide-Gunn Devices for Digital Circuits," Proc. Fourth Biennial Cornell Electrical Engineering Conf. 4:211-224, Cornell, Ithaca, New York (1973).
7. Pucel, R.A., Haus, H.A., and Statz, H., "Signal and Noise Properties of Gallium Arsenide Field Effect Transistors," Tech. Report No. R-73, Raytheon Co., Research Division, Waltham, Mass., 1974.
8. Hartnagel, H., Gunn-Effect Logic Devices, American Elsevier Publishing Co., New York (1973).
9. Sugeta, T., Tanimoto, M., Ikoma, T., and Yanai, H., "Characteristics and Applications of a Schottky-Barrier Gate Gunn Effect Digitized-Device," IEEE Trans. Electron Devices ED-21:8:504-515, August 1974.

10. Upadhyayula, L.C., "Trigger Sensitivity of Transferred Electron Logic Devices," IEEE Trans. Electron Devices ED-23:9:1049-1052, September 1976.

11. Upadhyayula, L.C., Smith, R.E., and Wilhelm, J.F., "Transferred Electron Logic Device (TELD) Development," Annual Report, Contract N00014-75-C-0100, RCA Laboratories, Princeton, NH

12. Hartnagel, H. L., "Theory of Gunn-Effect Logic," Solid-State Electron. 12:19-30 (1969).

13. Claxton, D.C., Leisher, T.D., and Mills, T.G., "TED BPSK Modulator/Demodulator Integrated Circuit Development," Final Technical Report, Contract N00014-76-C-0570, TRW Defense and Space Systems, Redondo Beach, California, February 1977.

APPENDIX A. TELD DEVICE MODEL

A computer model of the TELD was developed to predict the threshold conditions as a function of device and material parameters. The model is based on the one-dimensional model proposed by Pucel, et al,[A-1] for the FET. The program calculates the bias voltage across the TELD, the current through it, the voltage drop across the gate and the field in the channel at the threshold point. The program assumes a mature domain in transit and determines whether or not the bias voltage is greater than the sustaining voltage for the given geometry and material parameters.

Basic Equations:

ϕ = barrier height of the Schottky barrier gate junction

q = 1.6×10^{-19} coulombs

N_D = doping density in cm^{-3}

ε_0 = 8.854×10^{-14} f/cm

ε_r = dielectric constant of GaAs = 12.5

μ_n = carrier mobility $\sim$ 4500 cm/V-sec

E_s = velocity saturation field for GaAs $\sim$ 3.2×10^3 volts/cm

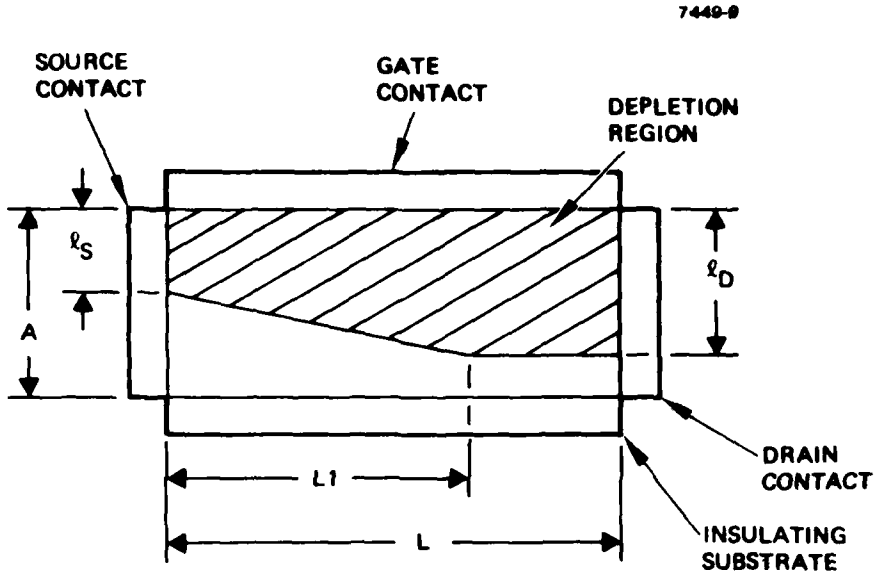
ω_0 is the gate to channel potential required to extend the depletion region completely across the channel, and is given by:

$$\omega_0 = \frac{qN_D}{2\varepsilon_r\varepsilon_0} A^2 \qquad \text{(A-1)}$$

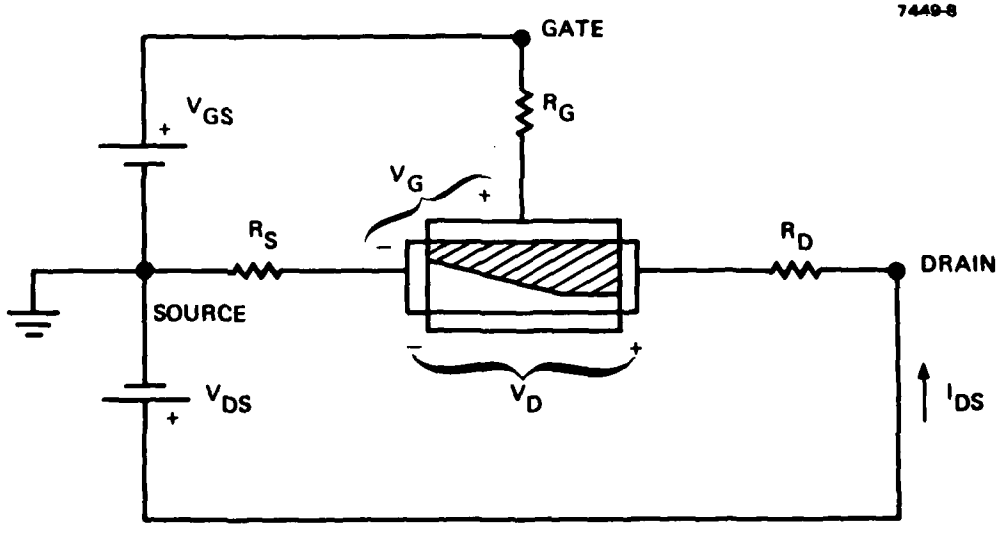
S is the fractional depleted channel width at the cathode contact (as shown in Figure A-1a) and is given by:

$$S = \frac{\ell_s}{A} = \sqrt{\frac{\phi - V_G}{\omega_0}} \qquad \text{(A-2)}$$

P is the fractional depleted channel width at the anode contact



(a)



(b)

Figure A-1. Cross-section diagram of FET used in computer simulation illustrating parasitic resistances and defining voltages.

(Figure A-1a) and is given by:

$$P = \frac{\ell_D}{A} \tag{A-3}$$

In the linear region of the I-V characteristics:

$$P = \sqrt{\frac{V_D + \phi - V_G}{\omega_0}} \tag{A-4}$$

In saturated operation, P must be solved by an iterative scheme. G_o is the undepleted channel conductance.

$$G_o = \frac{q\ \mu_n\ N_D\ AZ}{L} \tag{A-5}$$

where Z = gate width.

In linear operation, the anode current is given by

$$I_{AC} = \frac{G_o Z \omega_0}{L} \left[p^2 - S^2 - 2/3\ (p^3 - S^3)\right] \tag{A-6}$$

where P is as defined in equation A-4 and S is as defined in equation A-2.

In saturated operation above threshold, the equations become somewhat more complex. I_s is the current that would flow through the undepleted channel if all carriers traveled at saturated velocities.

$$I_s = G_o Z E_s \tag{A-7}$$

ε is a dimensionless parameter labeled the saturation index, give by:

$$\varepsilon = \frac{E_s L}{\omega_0} \tag{A-8}$$

The point L_1, at which velocity saturation first occurs is given by:

$$L_1 = L\left[\frac{p^2 - S^2 - 2/3\ (p^3 - S^3)}{\varepsilon\ (1-P)}\right] \tag{A-9}$$

And the anode current is given by:

$$I_{AC} = I_s\ (1-P) \tag{A-10}$$

where P must be determined to yield the proper V_D from the equation:

$$V_D = \omega_0 \left[p^2 - s^2 + \frac{2A\varepsilon}{\pi L} \sinh \left(\frac{\pi L}{2A} \left(1 - \frac{p^2-s^2-2/3\ (p^3-s^3)}{\varepsilon\ (1-P)} \right) \right) \right] \tag{A-11}$$

where S is as defined in equation A-2).

Method of Solution

It must be noted that all equations are derived in terms of the internal voltages V_A and V_G. Since the desired solution must be in terms of the externally applied voltages V_{AC} and V_{GC}, iterative calculations must be performend in order to find V_A and V_G consistent with the voltage drops across the parasitic resistances R_C and R_A. For the purposes of this program, the current through the gate contact has been assumed equal to zero and the gate resistance R_G neglected.

The parameter P has been redefined in order to avoid unnecessary duplication in the computer program. In the Pucel paper, P is defined as the fractional depleted channel width at $x = L_1$, the point in the channel where velocity saturation first occurs, and has no physical meaning in linear operation. In saturation, it is easily seen that P is equal to the fractional depleted channel width at the anode contact. It is assumed that the entire region from L_1 to the anode is velocity saturated. The channel current at L_1 may be expressed as:

$$I_{AC} = I_s\ (1-P) \tag{A-12}$$

and at the anode contact

$$I_{AC} = I_s \left(\frac{1-\ell_D}{A} \right) \tag{A-13}$$

Current continuity then implies:

$$I_s\ (1-P) = I_s \left(1-\frac{\ell_D}{A}\right) \qquad \text{(A-14)}$$

$$P = \frac{\ell_D}{A}$$

For convenience, this definition is also applied in linear operation.

A method of linear interpolation is used to determine the correct values of I_{AC}, P and S for given external voltages. Evaluation begins in saturated operation by guessing a value of P. I_{AC} is computed directly from equation A-12) and V_G determined by the relation:

$$V_G = V_{GC} - (I_{AC} \times R_C) \qquad \text{(A-15)}$$

This yields S from equation A-2 and V_D from equation A-11. The total anode to cathode voltage is finally calculated:

$$V_{AC} = V_D + I_{AC}\ (R_C + R_A) \qquad \text{(A-15)}$$

P is then either increased or decreased in increments of .01 until a span about the desired V_{AC} is obtained. A linear interpolation is next performed and the limits of the span are updated. This procedure is repeated until the desired accuracy is achieved.

After the dc operating point has been determined, L_1 is computed from equation A-9 to test for the transition to linear operation. When $L_1 > L$, the TELD is in linear operation and evaluation of the dc operating point now becomes somewhat more complex. As with saturated operation, a guess is made for P. I_{AC} is now a function of both P and S and a second interpolation loop must be added to determine S. A guess is made at the value of S, and I_{AC} computed from equation A-6. Re-arranging equation A-2 allows one to solve for V_G.

$$V_G = \phi - S^2\omega_0 \qquad \text{(A-16)}$$

and determine the external gate voltage

$$V_{GC} = V_G + (I_{AC} \times R_s) \qquad \text{(A-17)}$$

S is then increased or decreased in increments of .01 until a span is found about the desired V_{GC}, and a linear interpolation is performed as described earlier. Combining equations A-2 and A-4 allows computation of V_D

$$S = \sqrt{\frac{\phi - V_G}{\omega_0}} \qquad P = \sqrt{\frac{V_D + \phi - V_G}{\omega_0}}$$

$$\omega_0 S^2 = \phi - V_G \qquad \omega_0 P^2 = V_D + \phi - V_G$$

$$\omega_0 (P^2 - S^2) = V_D + \phi - V_G - \phi + V_G$$

$$V_D = \omega_0 (P^2 - S^2) \qquad \text{(A-18)}$$

V_{AC} is next determined by equation A-15. Solving for P continues as for the case of saturated operation with the exception that now, for each guess of P, the values of S, I_{AC}, V_{GC}, and V_{AC} must be computed as described above.

The program has a mode of operation in which only the transition point, the point at which the field reaches threshold under the gate, is calculated. This allows one to calculate a relationship between the threshold bias voltage and the gate bias. The results of the program for a structure shown in Figure A-1 are given in Table A-1. Figure A-2 relates the bias voltage to the normalized depletion depth. This relationship is independent of doping density. Only the value of X/d_o depends on the specific doping density for a given bias. The effect of doping density on X/d_0 is shown in Figure A-3. It is important in the design of TELD that the X/d_0 ratio be kept as small as possible. For ion implanted structures in which d_o is only $.5 \times 10^{-4}$ cm, this presents a severe limitation.

TABLE A-1. TELD THRESHOLD PARAMETERS

N_D cm^{-3}	V_{GC}, V	V Across Gate, V	V_{AC}, V	X/do	I_{AC}, ma
$1x10^{16}$	+0.5	.2734	3.044	.58	.47
	0.0	.2612	1.709	.78	.25
	-0.5	.2162	.677	.93	.08
$2x10^{16}$	+0.5	.2932	4.176	.42	1.33
	0.0	.2943	3.231	.56	1.0
	-1.0	.2870	1.837	.76	.53
	-1.5	.2768	1.265	.85	.34
$3x10^{16}$	+0.75	.2957	5.199	.27	2.52
	0.0	.3022	3.922	.46	1.86
	-1.0	.3015	2.786	.62	1.27
	-2.0	.2971	1.895	.76	.82
$4x10^{16}$	+0.5	.3034	5.002	.300	3.22
	0.0	.3058	4.337	.40	2.76
	-1.0	.3065	3.354	.54	2.09
	-2.0	.3052	2.583	.66	1.56
$5x10^{16}$	+0.5	.3056	5.214	.27	4.20
	0.0	.3080	4.621	.35	3.69
	-1.0	.3091	3.742	.49	2.94
	-2.0	.3088	3.053	.59	2.35

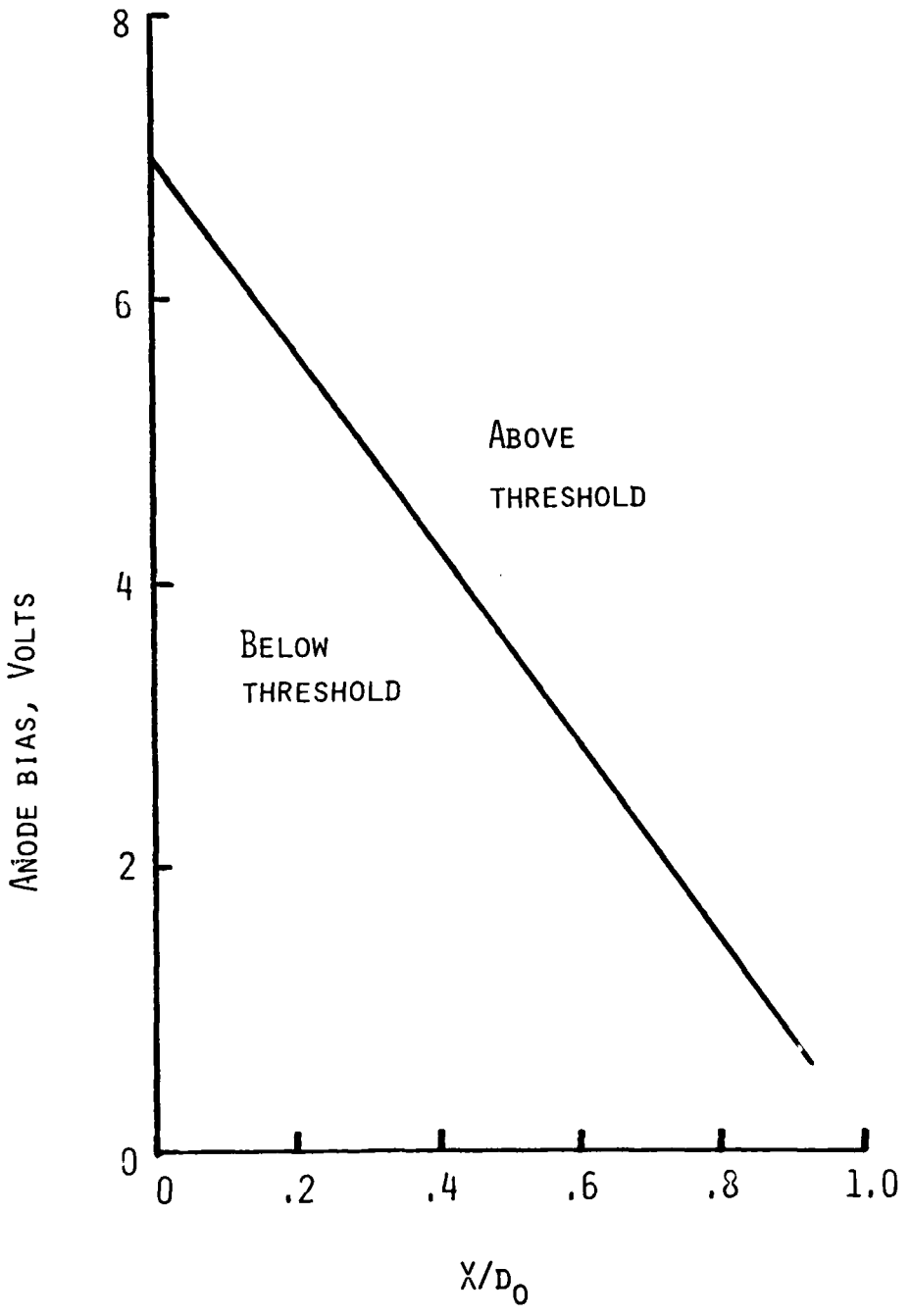


Figure A-2. Anode bias vs normalized depletion depth.

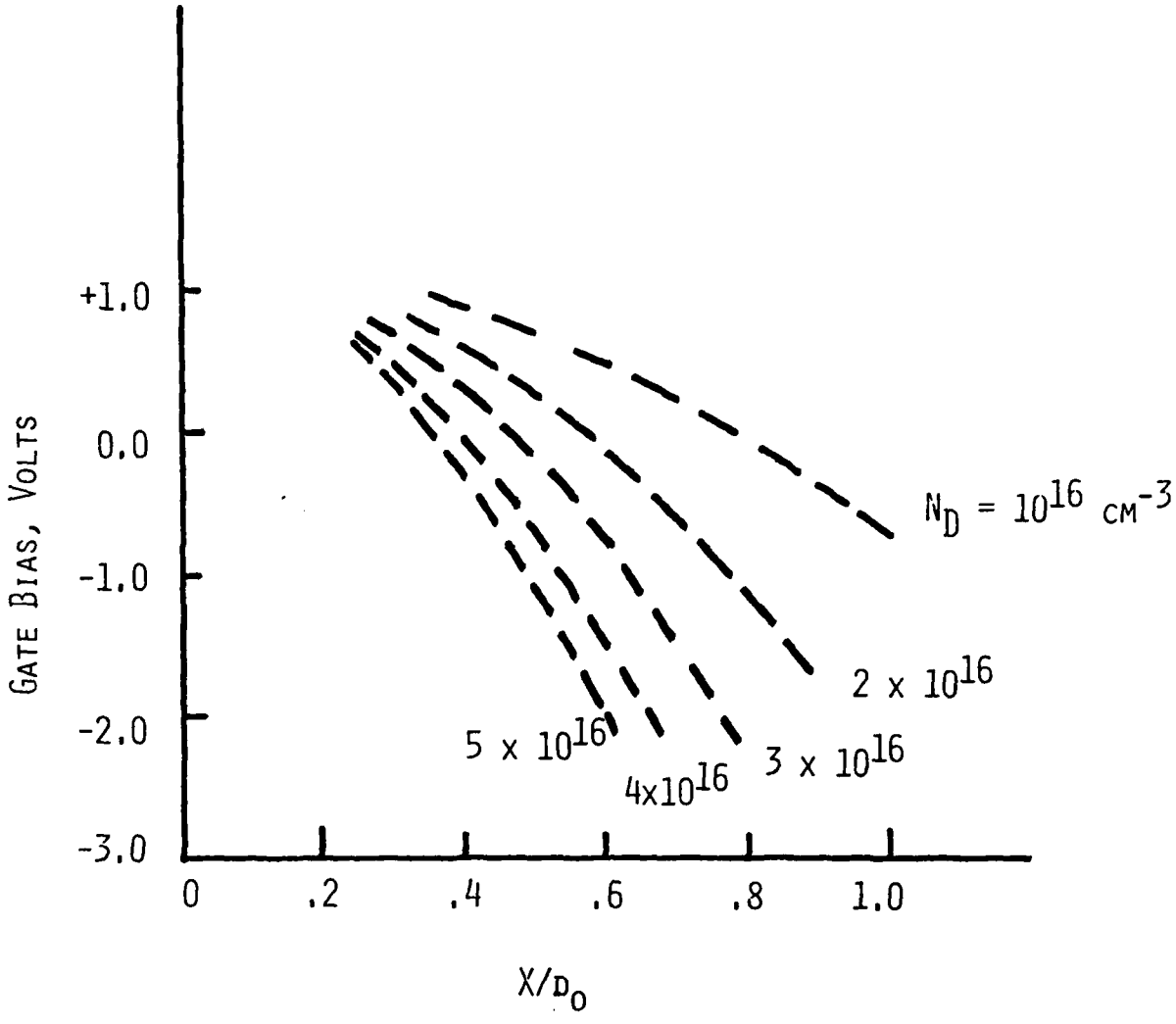


Figure A-3. Normalized depletion depth vs gate bias.

REFERENCES

A-1. Pucel, R. A., Haus, H. A., and Statz, H., "Signal and Noise Properties of Gallium Arsenide Field Effect Transistors," Raytheon Technical Report #R-73, September 1975.

APPENDIX B

Design of Ion Implanted TELD

An analysis is presented which investigates the important material parameters in the design of ion implanted TELDs. A first-order model for the device is proposed and analyzed with regard to the possiblity of domain formation and the amount of current "drop back" if the domain forms. The results of this model do show that with proper design of the implant and possibly some modification of the gate process, the theoretical conditions for domain formation are satisfied. This result has been verified experimentally[B1, B2].

The structure of a TELD is shown in Figure 2-1 (Section II) and will be referred to for the proposed model. In order to realize this structure by ion implantation, a double implant is necessary as shown in Figure B-1. Two requirements for domain formation are

$$N_d \ell_{gA} \geq 10^{13} \text{ cm}^{-2} \tag{B-1}$$

and

$$N_d \geq 10^{12} \text{ cm}^{-2} \tag{B-2}$$

as discussed previously (Section II).

The first constraint is obviously not satisfied in the tail of the implant since the doping density is too low. In this region a domain will try to form since the longitudinal field will be above threshold, however, the growth rate will be too low for a reasonable size domain to form. This region will load down the higher doped region where the domain is growing faster. Hartnagel[B3] suggests that this conductive load on the domain is similar to a dielectric load which is represented by a capacitor in shunt with the domain.

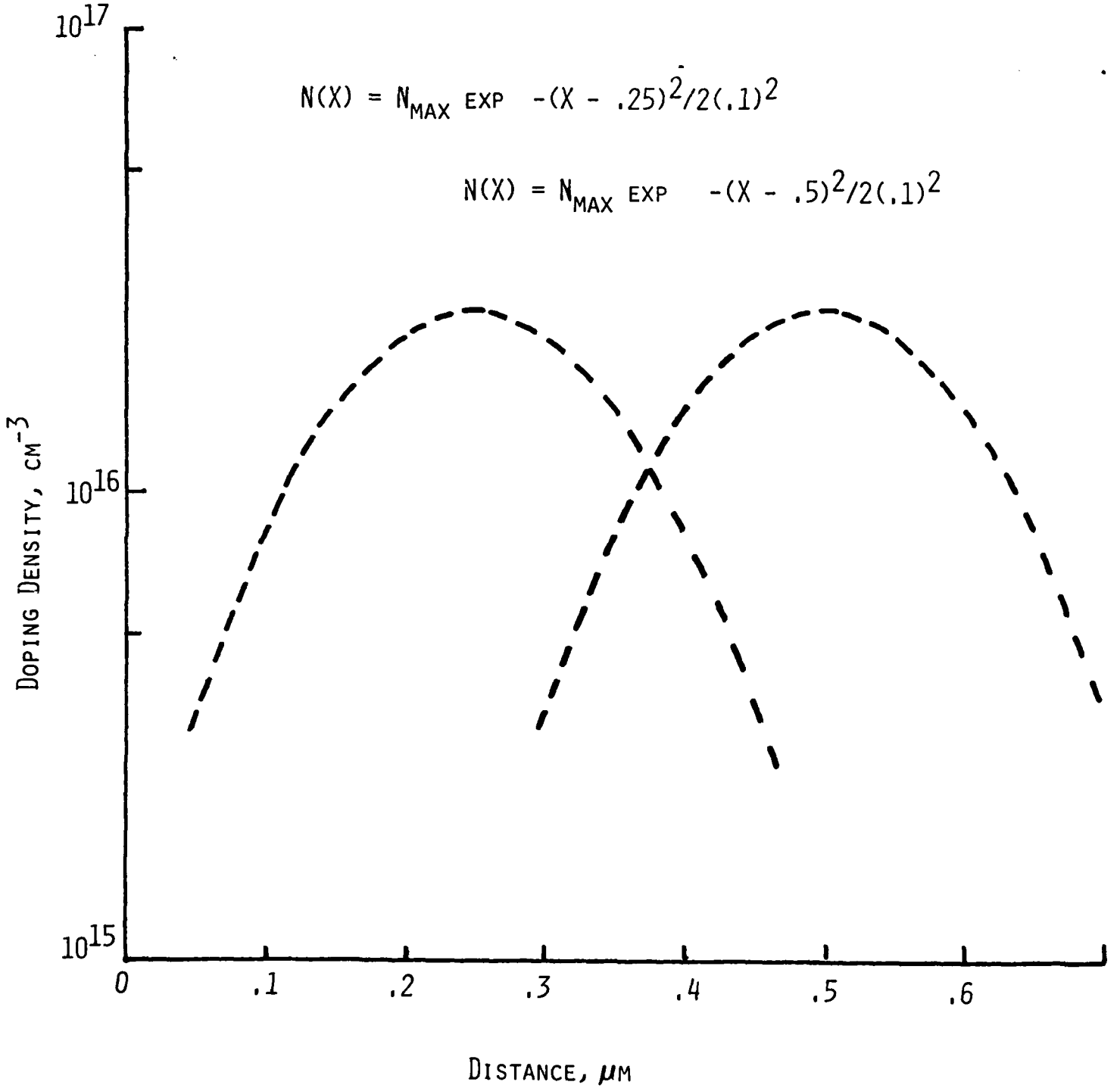


Figure B-1. Double implant doping profile for TED.

A similar problem exists in epitaxial material since the interface traps act as a resistance shunting the domain as it is in transit. Therefore, an equivalent circuit for the TELD is proposed as shown in Figure B-2. During domain growth the voltage across the equivalent domain capacitance is given by

$$V_D\ (t) = \frac{V_{bias}\ R_s}{R_o + R_s}\ (1 - e^{-t/\tau}) \qquad \text{(B-3)}$$

where

$$\tau = \frac{C_d\ R_s\ R_o}{R_o + R_s}\ .$$

Obviously the domain growth rate is strongly influenced by the shunt resistance.

In order to calculate the value of the shunt resistance, the mobility dependence on doping level was represented by the empirical formula[B-4]

$$\mu = \frac{7200}{[1 + 5.51 \times 10^{-17}\ N(x)]^{.233}} \qquad \text{(B-4)}$$

Therefore, the resistance of the implant tail is given by

$$R_S = \frac{\ell_d}{qb_o \int_{x_o}^{\infty} \frac{7200\ N_{max} e^{-(x-x_o)^2/2\Delta R_p^2}\, dx}{[\,1 + 5.51 \times 10^{-17} N_{max} e^{-(x-x_o)^2/2\Delta R_p^2}\,]^{.233}}} \qquad \text{(B-5)}$$

where x_o = the location of the implant maximum

and ΔR_p = range straggle

The resistance normalized to the domain width divided by the device width is plotted in Figure B-3 as a function of doping density for two values of ΔR_p. The normalized resistance of the low field region is plotted in Figure B-4 as a function of doping density for two values of ΔR_p. The domain capacitance is given by

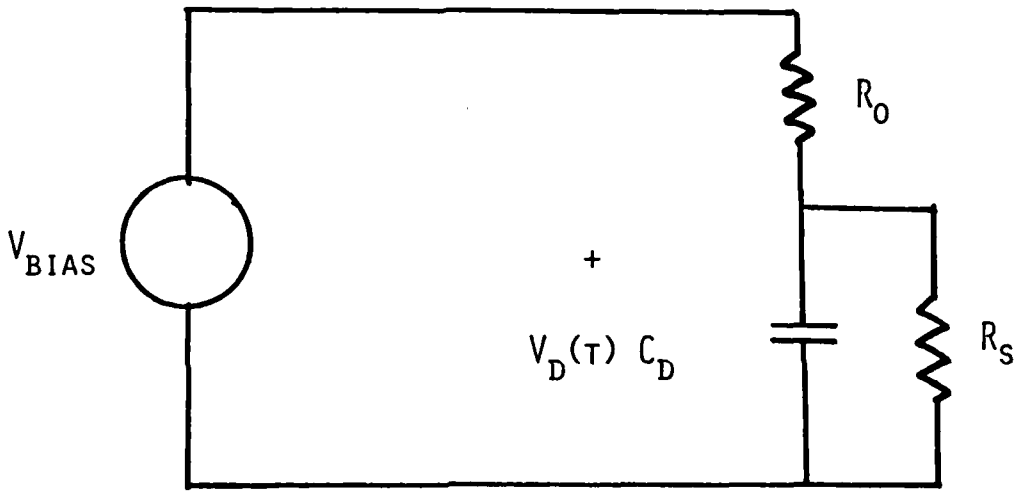


FIGURE B-2. EQUIVALENT CIRCUIT OF TELD

WHERE C_D = DOMAIN CAPACITANCE

R_O = LOW-FIELD RESISTANCE OF ACTIVE REGION AND IMPLANT TAIL

R_S = SHUNT RESISTANCE OF IMPLANT TAIL.

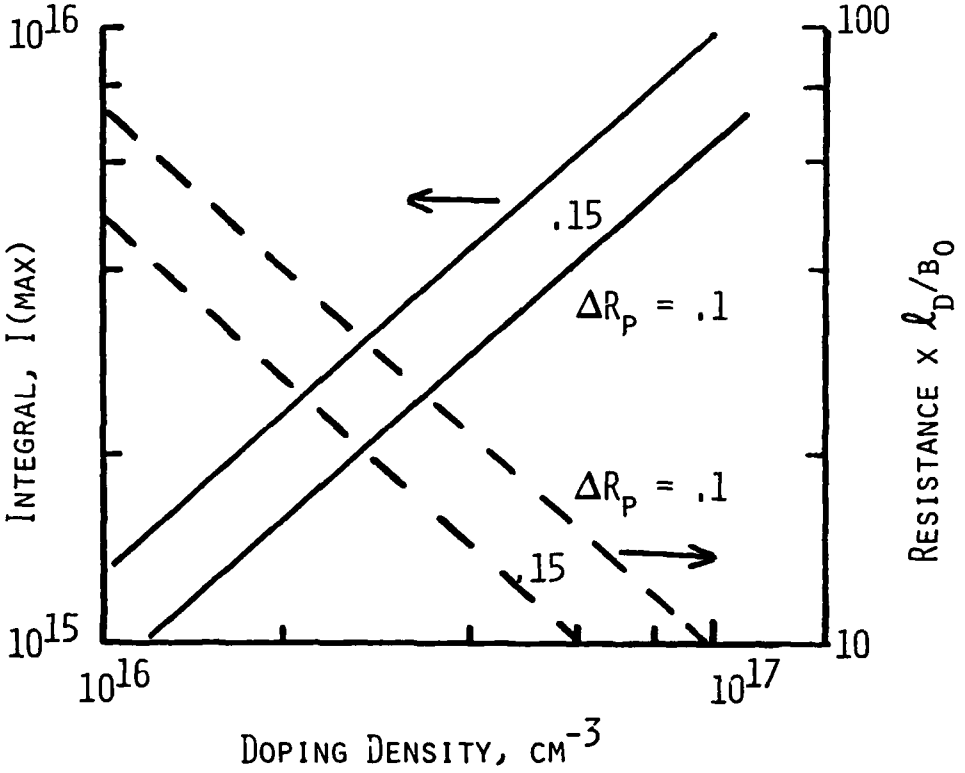


Figure B-3. Normalized resistance of implant tail.

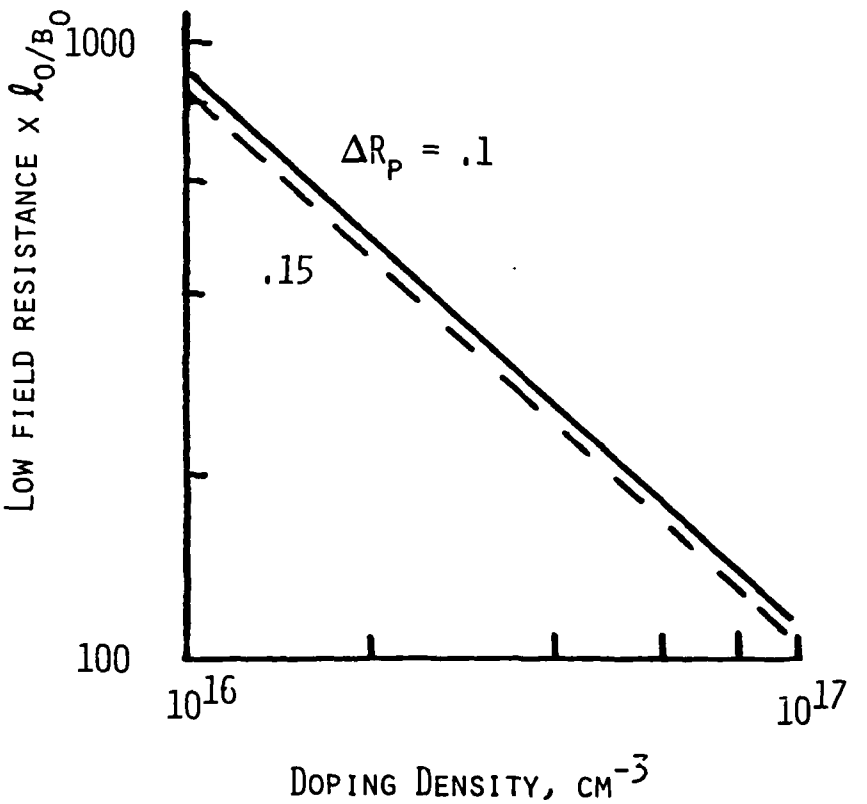


Figure B-4. Normalized low field resistance.

$$C_d = \frac{\varepsilon \text{ Area}}{\ell_d} \tag{B-6}$$

however, the domain width l_d, is a complex function of the device geometry and doping density. Also l_d is a function of time. As an approximation, the domain width is set equal to the active region depth.

Thus

$$\tau = \frac{C_d R_s R_o}{R_s + R_o} = \frac{\varepsilon d_o \bar{R}_s}{1 + \frac{\ell_d \bar{R}_s}{\ell_o \bar{R}_o}} \tag{B-7}$$

where $\bar{R}_s$ = normalized R_s and

$\bar{R}_o$ = normalized R_o.

In addition, the domain only charges to a value of $R_s/R_s + R_o$ or

$$\frac{R_s}{R_s + R_o} = \frac{1}{1 + \frac{\ell_o \bar{R}_o}{\ell_d \bar{R}_s}} \tag{B-8}$$

A plot of the domain voltage as a function of time is shown in Figure B-5 for the case of $N = 10^{16}$ and for an assumed ion implant range straggle of .1 and .15 μm. For comparison, the infinite shunt resistance is also shown.

The larger the domain voltage, the larger the current "drop back" or decrease. For an ideal TELD with a threshold velocity of 2×10^7 cm/sec and a high-field velocity of 1×10^7 cm/sec, the current would be reduced to 50% of its peak value. Normally workers measure 20-40% decrease or 80 to 60% of the threshold value. If the shunt resistance is included, the domain does not charge to as large a value and the current decrease is even less. Assuming the infinite shunt resistance case yields 50% final value, the effect of the shunt

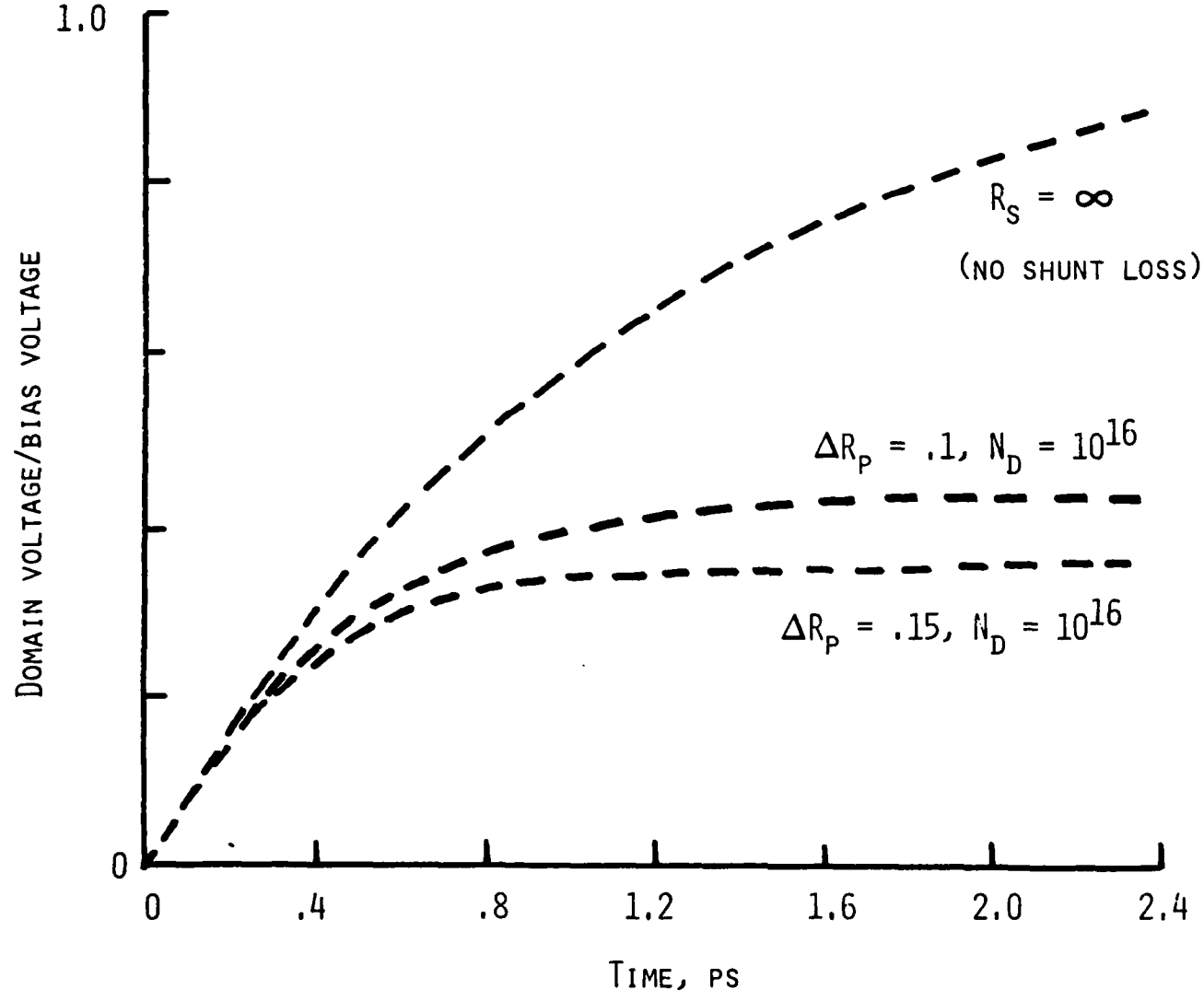


Figure B-5. Domain voltage vs time.

resistance on the final value is plotted in Figure B6 as a function of device length.

In order to satisfy the second constraint B-2, the doping density must be larger than 10^{16} for a 1 μm deep active region and 2×10^{16} for a .5 μm region.

Since the N_d d_o product is directly related to the current constriction under the gate, a possible solution is to extend the gate only part way across the TELD which reduces the effective depletion-layer. Another possible solution is to implant selectively under the gate a shallow, highly doped region in order to reduce the normal thickness of the depletion region.

An upper limit on the doping density is due to impact ionization in the domain. As N_d increases, the domain field becomes larger and it may be large enough for impact ionization to occur. A suggested upper limit is 1×10^{17} cm^{-3}, however, there is not experimental data to verify this value.

In conclusion, in order to realize a TELD by ion implantation a double implant will have to be used with a resulting doping density above 2×10^{16} cm^{-3} and below 1×10^{17} cm^{-3}. This will have to extend at least .5 μm into the GaAs. The tail on the implant should follow as nearly as possible the theoretical Gaussian implant profile level. In addition, a third implant under the gate may be necessary to minimize the zero-bias gate depletion region depth.

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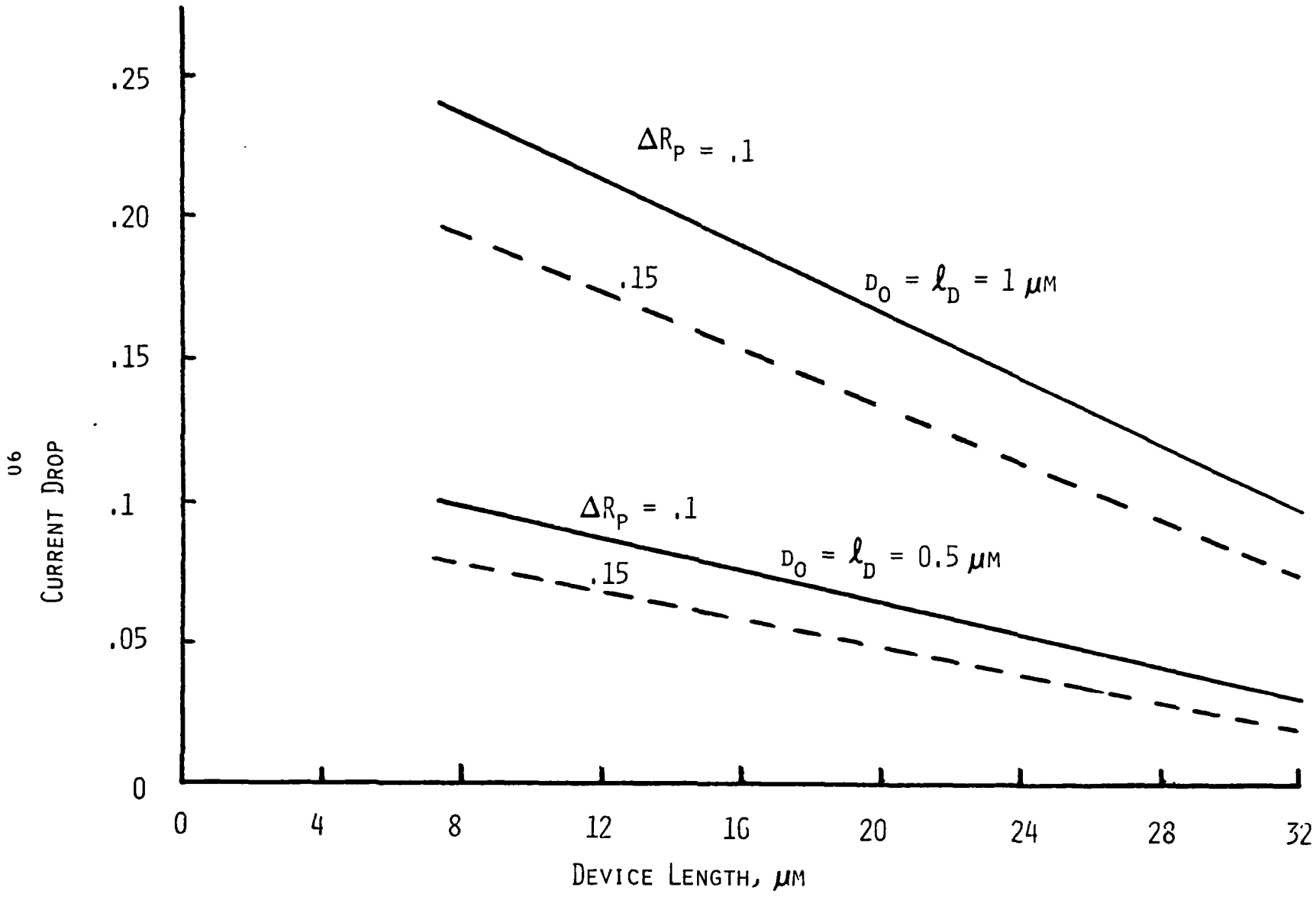

Figure B-6. Current decrease.

A-1. Yanai et al, 1976 Int. Microwave Sym. Cherry Hill, NJ, p. 161.

A-2. Metzutani et al, Elec. Lttrs., 11 Dec 1975, Vol. II, Nos 25/26.

A-3. Hartnagel Gunn-Effect Logic Devices, Amer. Elsevier Publishing C., New York 1973.

A-4. Harrison "Gallium Arsenide Technology", Vol. 1, Research Triangle Institute, Tech. Report AFAL-TR-72-312, Vol. 1, Jan 1973.

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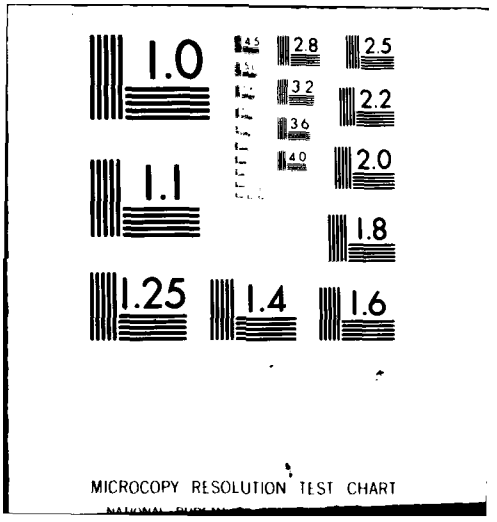
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